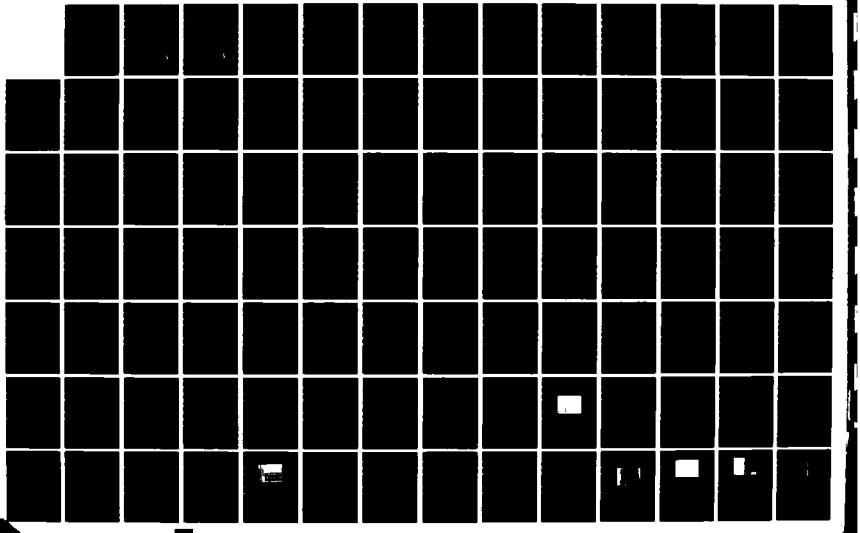
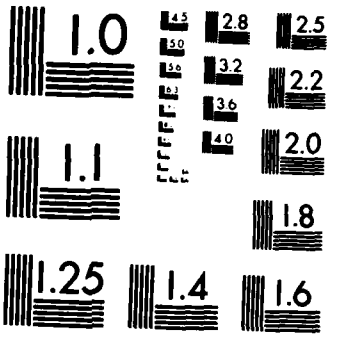
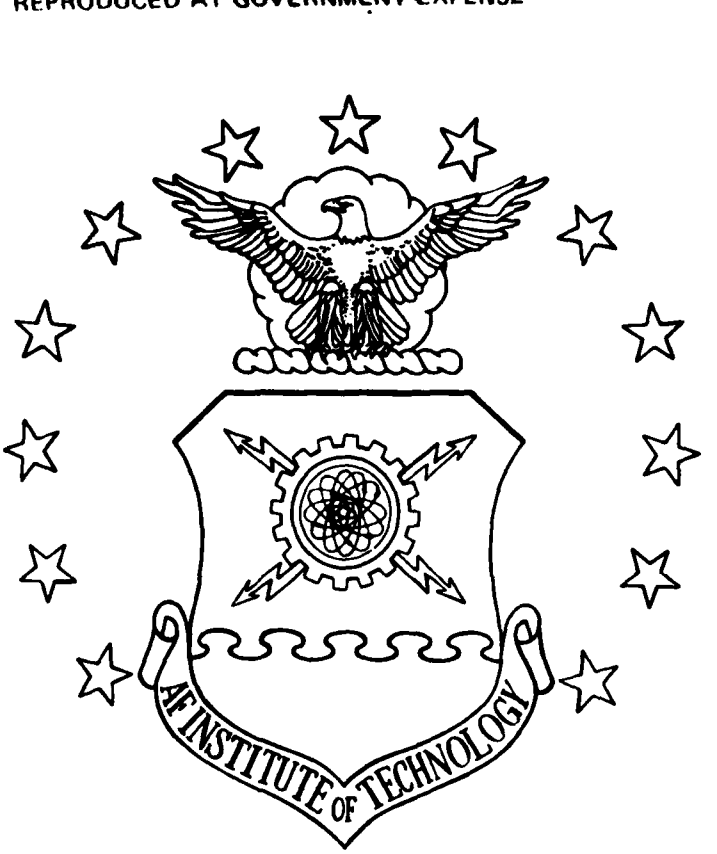
AD-A151 803 FABRICATION OF A BIOLOGICALLY-IMPLANTABLE MULTIPLEXED MULTIELECTRODE ARRA..(U) AIR FORCE INST OF TECH WRIGHT-PATTERSON AFB OH SCHOOL OF ENGI.. M E SOPKO 1/2

UNCLASSIFIED DEC 84 AFIT/GE/ENG/84D-63 F/G 9/1 NL







FABRICATION OF A BIOLOGICALLY-IMPLANTABLE, MULTIPLEXED, MULTIELECTRODE ARRAY OF JFETS FOR CORTICAL IMPLANTATION

THESIS

Michael E. Sopko
Second Lieutenant, USAF

AFIT/GE/ENG/84D-63

DEPARTMENT OF THE AIR FORCE
AIR UNIVERSITY
AIR FORCE INSTITUTE OF TECHNOLOGY

Wright-Patterson Air Force Base, Ohio

AFIT/GE/ENG/84D-63

FABRICATION OF A BIOLOGICALLY-IMPLANTABLE, MULTIPLEXED, MULTIELECTRODE ARRAY OF JFETS FOR CORTICAL IMPLANTATION

THESIS

Michael E. Sopko
Second Lieutenant, USAF

AFIT/GE/ENG/84D-63

Approved for public release; distribution unlimited

AFIT/GE/ENG/84D-63

FABRICATION OF A BIOLOGICALLY-IMPLANTABLE, MULTIPLEXED, MULTIELECTRODE ARRAY OF JEFETS FOR CORTICAL IMPLANTATION

THESIS

Presented to the Faculty of the School of Engineering
of the Air Force Institute of Technology
Air University
In Partial Fulfillment of the
Requirements for the Degreee of
Master of Science in Electrical Engineering

Michael E. Sopko, B.S.
Second Lieutenant, USAF

December 1984

Preface

The purpose of this thesis was to fabricate an implantable, multiplexed, multielectrode array of 256 JFETs based upon previous work by 2Lt J. A. Tatman, Capt G. H. Fitzgerald, Capt G. W. German, Capt R. W. Hensley, 1Lt D. C. Denton, and Capt Robert B. Ballantine. As a result of their individual and collective efforts, a semiconductor array suitable for implanting, monitoring, and recording visually evoked cortical signals has been developed and proven to be a viable research tool. The continued analysis of these recorded signals is crucial to understanding the principles by which the brain processes information.

This thesis is primarily concerned with fabricating and packaging a 16 by 16 multielectrode semiconductor array as a continuation of the work begun by Ballantine. Fabrication evolves around the development of a successful processing schedule using the work completed by Ballantine as a baseline. The device geometry is based upon the original Tatman mask design, but the arrangement now involves a 256 element JFET array as an improvement over the original 16 element array.

I gratefully acknowledge the advice and guidance provided by my thesis advisor, Capt Roger Colvin, during the course of this effort. Special thanks are also due to Capt Donald Kitchen, class advisor, and Mr. Donald Smith, electronics technician, for their continual suggestions, sup-

port, and encouragement in the laboratory. I also wish to thank Dr. Matthew Kabrisky for his valuable advice and inspiration, as a thesis committee member, in the preparation of this thesis. The sponsorship of the Air Force Aerospace Medical Research Laboratory is also acknowledged and greatly appreciated.

Michael E. Sopko

Table of Contents

List of Figures

List of Tables

Abstract

A new JFET multielectrode array, comprised of a 16 by 16 array of 256 junction field effect transistors, has been fabricated for use as a cortical implant. Changes in the fabrication procedure include: The use of a new chrome, six layer mask set, in lieu of emulsion masks; different diffusion times and temperatures; implementation of HCl gettering and backside gettering techniques; and a revised processing schedule incorporating different wafer cleaning procedures.

The primary emphasis of this study was on the development of a viable processing schedule for fabrication of the array. Secondary emphasis was placed upon interfacing the array to an NMOS multiplexer and a proposed method of mounting the device in a cortically implantable package.

FABRICATION OF A BIOLOGICALLY-IMPLANTABLE, MULTIPLEXED, MULTIELECTRODE ARRAY OF JFETS FOR CORTICAL IMPLANTATION

I. Introduction

Background

During the past several years, AFIT professor Dr. Matthew Kabrisky has been engaged in investigations of the pattern recognition process used by the visual imaging mechanism of the human brain. Current medical methods, such as the Electro-encephalogram or EEG, used to measure and study the electrical activities of the brain have been proven inadequate for this research. These methods do not provide a precisely localized measurement of the actual processes that occur in the portion of the brain associated with visual perception. Utilization of methods such as the EEG to study the signal processing of the brain can be compared to "trying to determine the inner workings of a digital computer by measuring the magnetic and electric fields surrounding it during operation."

Kabrisky and others have theorized that the cerebral cortex of the brain is comprised of bundles of neurons forming functional units called basic computing elements or BCE's (Ref 1:40). The BCE's of the visual cortex are on the order of 50 microns and are thus difficult to probe on an individual basis due to the small size required of any conventional electrodes which could be implanted at the surface of the brain. Electrodes of microfine dimensions

and dense spacing are essential if any detailed measurements of visual perception are to be obtained.

In a 1979 thesis effort at AFIT, Lt. Joseph Tatman proposed a method of measuring electrical signals at the surface of the brain which met the size and accuracy constraints posed (Ref 2). Tatman's scheme involved the fabrication of a silicon integrated circuit chip consisting of: (a) an electrode array (n-rows by m-columns) expandable to several thousand electrodes with dedicated junction field effect transistors (JFET's) functioning as on/off switches for each electrode, (b) matrix multiplexing the array to a single output, and (c) outputting the data across an intact scalp by using a low power tunnel diode RF transmitter. Tatman designed and fabricated a four by four electrode array with sixteen JFETs which utilized five wires for power and control, and four signal wires to convey data through an opening in the scalp. The design was basically an initial prototype for follow-on efforts, however, Tatman's trial fabrication run failed to yield any working devices.

A 1980 follow-on effort by Capt. Gary H. Fitzgerald (Ref 3) involved a revision of Tatman's processing schedule and did result in a device which functioned. However, the device did not function properly in simulated cerebrospinal fluid (a saline solution), which was to be the eventual environment of the chip.

Capt. George W. German (Ref 4), in a 1981 thesis project, succeeded in developing a suitable passivation

layer to protect the chip from sodium ions that are fatal to the operation of the integrated circuit chips. German was able to exercise one of the Fitzgerald chips in a saline bath for an extended time before the device failed.

Finally, in 1982 Capt. Russel Hensley and Lt. David Denton (Ref 5) were able to provide some preliminary insight into the imaging mechanism when a silicon integrated circuit chip with an array of 16 electrodes was medically implanted at the surface of the brain of a live dog. The effort was successful and much useful information was obtained, however, the implanted device failed after 19 days of operation. Additional research of this type is still being planned and the development of an implantable device which is capable of reliable operation for a sustained period of time is of paramount importance for the continued success of future research efforts in the areas of visual perception and pattern recognition.

Statement of Problem

The electrode array which was successfully implanted in the dog was composed of a 4 by 4 matrix or array of 16 Junction Field Effect Transistors (or JFETs as they are commonly referred to). A major problem encountered with the device was a non-uniformity of the sensitivity of the individual matrix elements. It is believed that this deficiency may be corrected through careful processing during the fabrication of the device. Since the JFET structure is

inherently vulnerable to sodium contaminants, extra precautions must be instituted to ensure its successful operation.

There are several factors which contribute to the difficulty of maintaining the reliability of an electronic device implanted in a living mammal. One of the most detrimental conditions is the fact that the device must operate in a saline environment, i.e. in surrounding fluids which contain a high sodium content. Sodium happens to be a very mobile ion that is capable of diffusing into the active layer of the integrated circuit chip and is fatal to the operation of integrated circuits. Therefore, any device suitable for long term use must be "passivated" against the harmful effects of operating in this harsh environment.

Passivation entails the application of a protective coating to shield the device from the sodium contaminants and yet enable it to function correctly. The chip to be developed must be suitably passivated and tested to be reliable for long term use. It must also produce uniform outputs which provide an accurate indication which is representative of the signals being measured. Additionally, it is desired that a measuring device have greater resolution than that associated with the previous endeavors which utilized a four by four array. Thus an array composed of more elements and smaller dimensions is required. Finally, to reduce the number of wires required for control of the array,a multiplexer chip will also be located in the implantable package.

Scope

It is proposed that an electrode array similar to the one which was successfully implanted in the dog be developed, fabricated, packaged, and fully tested to insure its reliability under the intended operating conditions. These conditions will be simulated by a saline environment while reading electrical signals comparable to those encountered at the surface of a brain. The main emphasis of this thesis effort involves five major areas, each delineated as follows.

The first area is the determination of causes for the failure of Capt. Robert Ballantine (Ref 6) to produce functioning devices by the processing schedule used in his 1983 AFIT thesis. These shortcomings will be eliminated by producing a revised processing schedule. The second area involves the reduction of leakage current by introducing processing innovations, such as backside gettering and the presence of HCl during oxide growth, which not used in the previous processing attempts. A third area is the duplication and reversal of the passivation (Layer 6) mask since it is for use with negative photoresist rather than positive photoresist. The fourth area includes the actual fabrication and testing of the 16 by 16 array. The final area encompasses interfacing an NMOS multiplexer chip, which was developed by Ballantine (Ref 6), to the 16 by 16 array, passivating the array, and then mounting the entire unit in a package developed by Capt. Ricardo Turner in a concurrent

1984 AFIT thesis effort (Ref 7).

It is not proposed that this thesis effort be a repeat of previous work. Steps will be taken to optimize the electrode array to be fabricated by utilizing information gained from past attempts and eliminating previous errors and shortcomings. The electrode array to be fabricated will be composed of a 16 by 16 array of JFETs fabricated on a silicon substrate. The "source" of each JFET will form the individual sensing electrodes. The "drains" will carry the sensed signals to an external recording device, and the "gates" will be driven by a previously fabricated NMOS multiplexer chip. The packaging of the final functional device will be an entirely new development. An attempt will be made at packaging the device in an appliance similar to a hollow bone screw. The package will be suitable for mounting in the skull of a rhesus monkey and be passivated and tested in preparation for implantation. This thesis project will not, however, involve the implanting of a device in a biological specimen, nor will it involve the recording or analyzing of any biological data.

Assumptions

Since the first attempt at implanting an electrode array was successful with the implementation of a 4 by 4 matrix of 16 JFETs in a dog, it will be assumed that this same technique is still applicable to the proposed method of interfacing an NMOS multiplexer to a 16 by 16 array of 256

JFETs. Further, it will be assumed that a working NMOS chip will be available. It will also be assumed that the previous passivation technique of encapsulation with polyimide is adequate for the intended purpose, but this premise will be subject to intensive testing after a working device is fabricated.

Summary of Current Knowledge

As was previously mentioned, the sensing method proposed in this effort has already been tried successfully, and modifications developed in this thesis should primarily serve to enhance the findings of past attempts. The most recent work completed on the "AFIT Brain Chip", as it is now commonly referred to, was by Capt. Robert Ballantine in a 1983 thesis effort. The areas of Ballantine's work applicable to this thesis included: the design of a multiplexer chip to be commercially fabricated using NMOS technology; the layout of a new 16 by 16 JFET array mask set; the revision of Fitzgerald's processing schedule; and an actual trial fabrication run to produce functional four by four JFET arrays using "reversed-sense" (dark field as opposed to light field) Tatman masks.

Due primarily to processing difficulties, Ballantine unfortunately failed to produce any functional JFETs. The JFETs were fabricated on three-inch silicon wafers having two micron epitaxial layers with nine chips on each wafer. From subsequent analysis of Ballantine's work, it was deter-

mined that the processing schedule followed resulted in the gate region diffusing completely through the epitaxial layer and into the wafer substrate, thus forming FETs that were permanently fixed in the pinched-OFF mode. It is believed that the failings of this previous attempt can be resolved.

Standards

The electrode sensing array to be fabricated must be sensitive enough to measure signals on the order of 50 to 1000 microvolts (Ref 5:A-1) since this is typical of the signals found on the surface of the brain. It is also desired that the passivation layer retain its integrity for a period of time on the order of one year. The package to be developed for the device must practical in the sense that it can be mounted in the skull of a rhesus monkey and provide adequate sensing of electrical impulses on the surface of its brain. In addition, it must allow for non-surgical insertion and removal of the chip after the initial surgery for the chronic implant of the mount has been performed.

Approach

After careful evaluation, the causes for the failure of the previous attempt by Ballantine to fabricate a JFET array will be eliminated by modifying the processing schedule which he used. The revised processing schedule should be designed to maximize signal sensitivity and immunity to processing defects. Techniques for protecting against sodium ion contamination, in both fabrication and operation,

will also be investigated. A brief schedule of the development is as follows:

(1) Trial oxide growth and evaluation using C-V plots
(2) Trial diffusions and evaluation by bevel & stain and resistivity measurements
(3) Revision of processing schedule
(4) Trial exposures of photoresist on 3" wafers using new mask set
(5) Actual device processing
    a) Multiple runs for gate diffusion
    b) 2 layer metallization -- silver on top of aluminum
(6) Polyimide passivation
(7) Saline environment testing
(8) Packaging and testing of final practical device

Every effort will be made to maintain an adherence to Ballantine's processing schedule as much as possible, with revisions being made only to correct fabrication deficiencies, rather than developing an entirely new processing sequence that would involve a high probability of new deficiencies preventing successful device fabrication before the graduation deadline.

Sequence of Presentation

This thesis is primarily geared toward the fabrication of the 16 by 16 JFET array, and the presentation is oriented toward a chronological development of the processing schedule used in actual fabrication of the device. Ballantine's thesis is used as a baseline from which the development of this thesis proceeds.

Chapter II presents the analysis of the field oxide. This analysis includes growth kinetics and evaluation of the quality (cleanliness) of the grown oxide through capacitance-

voltage (C-V) testing. The advantages of HCl ambient during oxide growth and the technique of backside gettering are also discussed.

Chapter III presents the diffusion trials performed to determine correct deposition and drive times required to arrive at the initial concentration and depth values determined by Ballantine. The supporting calculations for all diffusions are also included in Chapter III. These results are combined with those arrived at by Ballantine, and from the conclusions drawn, a revision of the processing schedule used by Ballantine is derived as an initial processing schedule to be followed in this thesis.

Chapter IV presents the chronological steps associated with the actual fabrication runs. Considerations for revision of the initial processing schedule are also included and explained in the chapter.

Chapter V presents the results of electrical tests on the array using a transistor curve tracer and the results obtained by bevelling and staining the final devices. An analysis of the test results is also included.

Chapter VI presents the passivation procedure and the method of interfacing the JFET array with the multiplexer chip developed by Ballantine. It also discusses the actual mounting and packaging of the complete multiplexer/ passivated-array unit.

Chapter VII presents conclusions derived from the actual fabrication and recommendations concerning future

processing.

In addition, material is presented in the appendices which is pertinent to this thesis, but is either too detailed or too insignificant to be included in the main text.

II. Analysis of Oxide Cleanliness

Introduction

It was decided the most logical starting point prior to actual device processing was to determine whether or not the proposed fabrication facilities of the AFIT/ENG Cooperative Education Laboratory in Building 125 met minimum cleanliness standards. In the event this facility proved to be inadequate, the possibility of using an alternate production site would have to be investigated. Arrangements could be made to use the Semiconductor Processing facilities at the Avionics Laboratory.

As an indicator of the level of cleanliness in the Co-op Lab, Capacitance-Voltage (C-V) characteristics of test oxides grown in the laboratory were examined. In addition, these test oxides were used to check the operation of the diffusion furnace oxidation tube by comparing measured thicknesses of the oxide against calculated values.

Oxide Growth

Thermal oxidation of silicon through the following chemical reactions was the method used to grow the necessary test oxides as well as subsequent oxide masks during actual device processing (Ref 8: 22):

"dry"

$$Si(solid) + O_2 \longrightarrow SiO_2(solid) \qquad \text{(II-1)}$$

"wet"

$$Si(solid) + 2H_2O \text{ ----> } SiO_2(solid) + 2H_2 \quad \text{(II-2)}$$

As oxide is grown through these reactions, the silicon on which it is formed is consumed during the process. Approximately 45 percent of the total oxide thickness grown is contributed by the original silicon surface (Ref 8: 23). This fact must be accounted for when performing calculations concerning diffusion depths because the distance the dopants must diffuse through is reduced during prior oxidation. The oxide growth rate yielded by Eq (II-2) is an order of magnitude greater than that which is produced by Eq (II-1), however the oxide produced by Eq (II-1) is much denser (less porous) and initially grows at a faster rate than that of Eq (II-2).

Initial adjustments made prior to using the diffusion furnace included: (1) profiling the oxidation tube to 1050° C (see Appendix A), (2) adjusting the N_2 and O_2 gas flows to 1.0 liter per minute and one atmosphere of pressure, and (3) adjusting the steam bubbler controller such that it maintained a liquid temperature between 95 and 100 degrees C. Five, three-inch test wafers were then cleaned using the Standard Processing Clean (see Appendix K) and placed in the oxidation tube of the diffusion furnace. The wafers used are identified and described in Table II-1.

Table II-1. Test Wafer Identification and Description

WAFER ID NUMBER	TYPE Epi/Subs	EPI RESISTIVITY ρ, Ω-cm	EPI LAYER THICKNESS t_{epi}, μm
D-1	N/P	0.81 - 0.99	1.8 -2.2
D-2	N/P	0.95	2.0
S-1	N/P+	1.0	4.1
S-2	N/P+	1.0	4.1
CV-1	N/N	1.0	4.1

The initial goal of oxide thickness was 2500 angstroms and the time required to produce this growth, using a combination of wet and dry oxidation periods, was calculated using graphical data (Ref 17: 92-93). The results arrived at are shown in Table II-2.

Table II-2. Summary of Actual Oxide Thickness Grown

WAFER ID NUMBER	MEASURED OXIDE THICKNESS angstroms, A	DRY GROWTH PERIOD minutes @ 1050°C	WET GROWTH PERIOD minutes @ 1050°C
D-1	2400	20.0 + 20.0	10.0
D-2	2390	"	"
S-1	2335	"	"
S-2	2300	"	"
CV-1	2410	"	"

Cleanliness Evaluation by C-V Testing

One of the most common and detrimental contaminants to semiconductor devices is the sodium ion. Because sodium is extremely mobile in silicon, the sodium ions are free to migrate throughout the crystal lattice acting as charge carriers which give rise to gross leakage currents through the device. If large enough, these currents can render a

device useless.

Since sodium is so prevalent an element, it is exceedingly difficult to eliminate it from the processing environment. Gross concentrations of sodium are found on the skin (perspiration), in tap water, and on laboratory utensils. Since these are all commonly used objects, they serve to distribute the sodium contaminant throughout the laboratory. The principal means, however, by which sodium contamination is introduced into a silicon wafer is during high temperature processing -- since the diffusion coefficient is higher, ions are more mobile and diffuse more readily into the silicon wafer. Sodium enters the processing ambient by diffusing through the quartz walls of the diffusion tubes. One highly effective method of cleaning ("gettering") the quartz diffusion tube of sodium ion contamination is to etch the walls of the tube using HCl (or similar chlorine-bearing compound) as a gas purge lasting several hours prior to use (Ref 3: 50).

The following prescribed method of obtaining a C-V plot can be used to evaluate the presence of mobile ions in the silicon dioxide layer (Ref 9: 49-56; 10: 46-55). A C-V test is first performed at room temperature. The wafer is then heated to a temperature of 150 to 300 degrees C for one minute to three hours while a dc bias of 10 volts per 1000 angstroms of oxide is applied. This bias/temperature stress causes the mobile ions to drift under the influence of the electric field produced by the dc bias. With the dc bias

removed the C-V characteristic is measured again. An example of a typical C-V plot thus obtained is detailed in Figure I.

The voltage shift along the horizontal axis is directly proportional to the concentration of mobile ions present in the oxide. For a given BT, a greater voltage shift (corresponding to a set capacitance) indicates a higher concentration of mobile ions. Knowing the oxide thickness, the oxide capacitance can be calculated using the equation (Ref 6: III, 10):

$$C = \epsilon_o \epsilon_r A d^{-1} \qquad \text{(II-3)}$$

where

C is capacitance in farads, F,

d is oxide thickness in meters, m,

$\epsilon_o = 8.854 \times 10^{-12}$ F-m^{-1}, is the permittivity of free space,

$\epsilon_r = 3.9$ is the relative dielectric constant of silicon dioxide, and

$A = 8.11 \times 10^{-7}$ m^2, is the area of the aluminum dot (Ref 6: III, 10).

From the measured voltage shift and capacitance, the actual concentration of mobile ionic contaminants may be determined. Approximately 10^{10} to 10^{11} charges per cm^2 constitutes a relatively "clean" oxide, whereas a relatively "dirty" oxide is characterized as having between 10^{11} to 10^{14} charges per cm^2 (Ref 9, 10, 11).

For each one volt of shift over an oxide 2000 angstroms thick, approximately 10^{11} charges per cm^2 are drifted. The charges drifted obey a linear relationship, e.g. a two volt shift for an oxide 4000 angstroms thick is equivalent to the aforementioned charge concentration drifted. Commercial industry attains cleanliness standards of 0.1 volt shifts corresponding to $2x10^{10}$ charges per cm^2 drift for oxide thicknesses of 1000 angstroms, where the BT stress applied is (Ref 9, 10, 11):

B = $2x10^6$ V-cm^{-1} of oxide thickness
T = 300 degrees C for 5 minutes.

Prior to performing the C-V testing, an aluminum dot pattern was deposited over the entire oxide surface of wafer CV-1 (see Table III). The metallization was performed by placing the wafer in a vacuum vapor deposition chamber with a stainless steel shadow mask between the oxide surface and the evaporation source. The mask comprised a matrix of holes 40 mils in diameter on 50 mil centers. The deposition was performed as per the manufacturer's operating instructions (Ref 12, 13) resulting in the desired aluminum dot pattern (3000 angstroms thick) being placed on the oxide surface. Each dot acts as one plate of a parallel plate

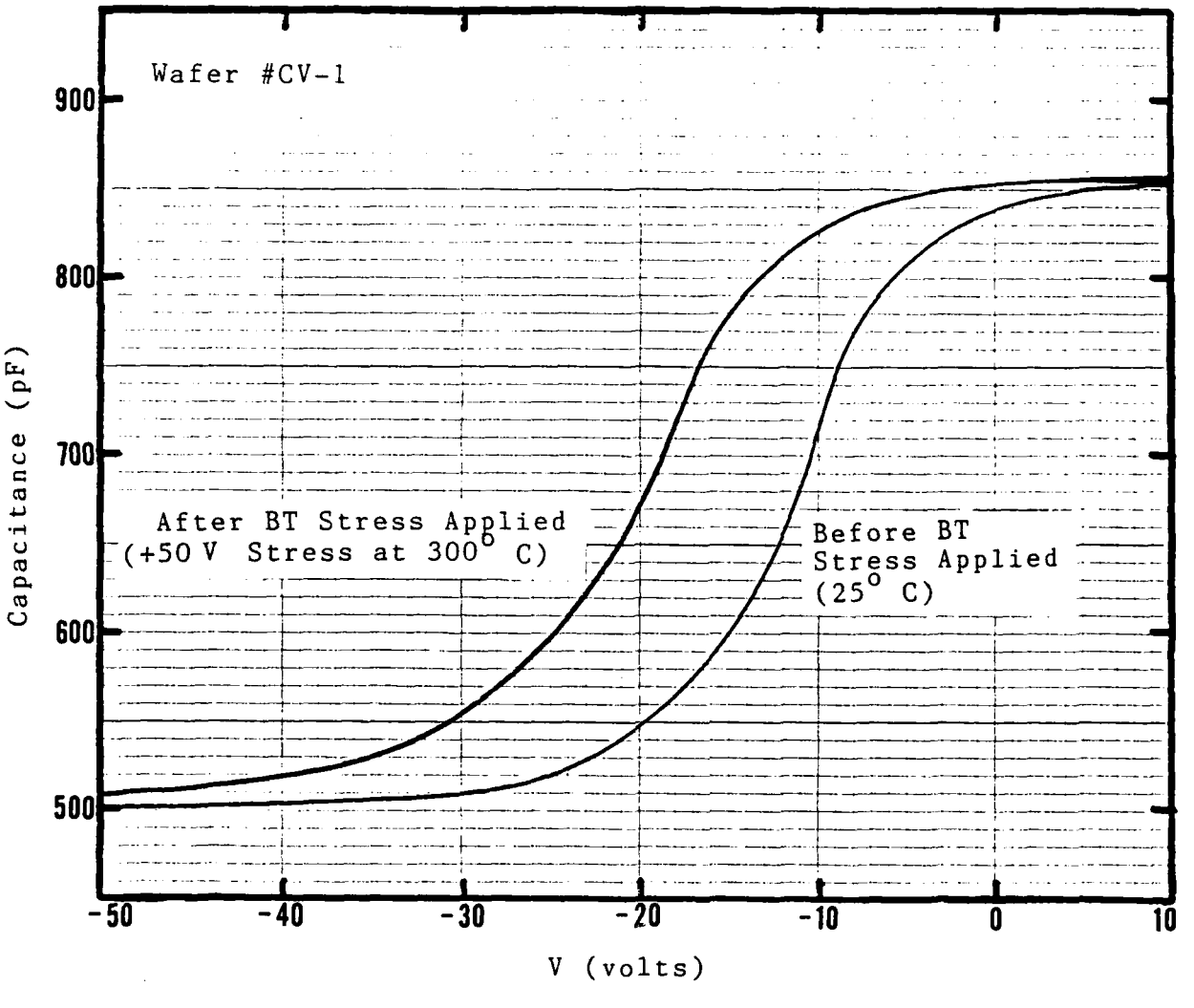


Figure II-1. C-V Characteristic Plot

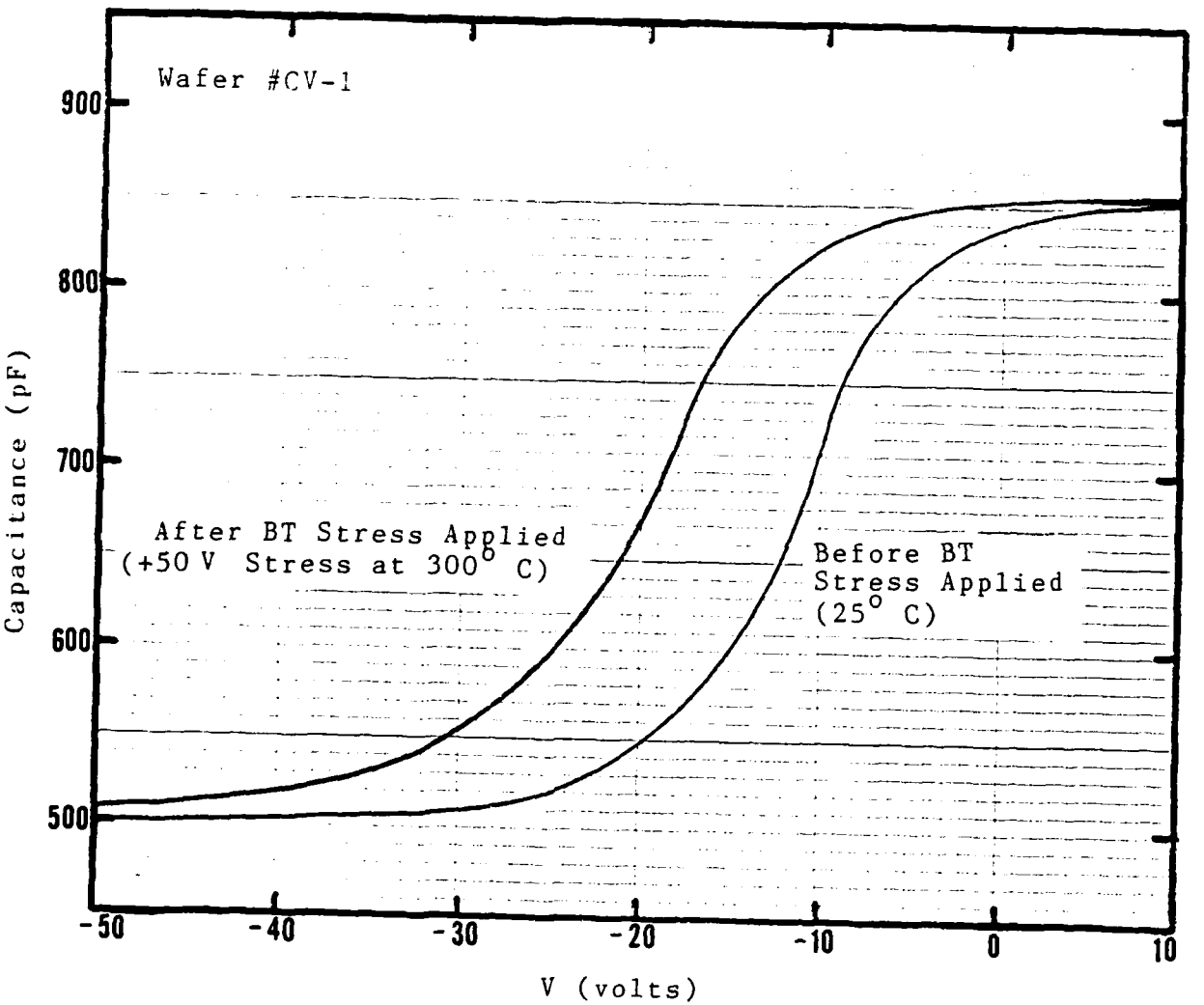


Figure II-1. C-V Characteristic Plot

capacitor with the oxide forming the dielectric, and the silicon substrate (epitaxial layer actually) acting as the accompanying plate. The evaporated metallization layer was then annealed at 500 degrees C for ten minutes to toughen the dots thus enabling them to withstand being probed as electrodes during C-V test procedures. The wafer (CV-1) with n-type epi layer and type n+ substrate was selected for the C-V test to avoid the inaccuracies which would have arisen from the epi/substrate p-n junction capacitance present had a type n on p+ wafer been used.

Using the information available for the C-V Plotter (Ref 14), a C-V test was performed on wafer CV-1. In order to meet the previously mentioned stress requirement of 2×10^6 V-cm^{-1} on an oxide 2410 angstroms thick, a positive 50 volt dc bias, referenced to the substrate, was applied to a metal dot on the wafer surface with the ramp start and stop voltages set to +50 volts and -50 volts respectively. A C-V plot was then obtained at room temperature. The wafer was then heated to 300 degrees C and held at that temperature for 15 minutes with the dc stress bias still applied, and another C-V characteristic curve was plotted. The results obtained are shown in Figure II-1.

Substituting an oxide thickness of 2410 angstroms into Eq (II-3) gave a capacitance of 116.2 pF. From the 8 volt shift shown by the plot, the mobile ion concentration present was concluded to be approximately $6 - 7 \times 10^{11}$ cm^{-2}, as is supported by the following calculations:

$$C = \epsilon_o \epsilon_r A d^{-1}$$

$$= \frac{(8.85\times10^{-12})(3.9)(8.11\times10^{-7})}{2410\times10^{-10} \text{ coulombs}}$$

$$= 116.2 \text{ pF} \qquad \text{(II-4)}$$

$$\Delta Q = C \Delta V \qquad \text{(II-5)}$$

$$Q = (116 \times 10^{-12})(8)$$

$$= 9.3 \times 10^{-10} \text{ coulombs} \qquad \text{(II-6)}$$

The concentration of mobile ions in the oxide is calculated as

$$N_{ions} = \frac{Q}{qA} = \frac{9.3\times10^{-10}}{(1.6\times10^{-19})(8.11\times10^{-3})} \qquad \text{(II-7)}$$

$$N_{ions} = 7.2 \times 10^{11} \text{ cm}^{-2} \qquad \text{(II-8)}$$

Although this number is slightly greater than what constitutes a "clean" oxide, the contaminant level should be low enough that functional JFETs could be fabricated in the lab if the following described corrective procedures are instituted.

Corrective Innovations

HCl Gettering. One of the techniques implemented during actual device processing to substantially improve the quality of the oxide grown was the use of HCl gettering during oxide growth (Ref 15, 16). This technique entails the introduction of HCl into the oxidizing ambient. The presence of HCl in the oxidizing gas exhibits the effect of cleaning ("gettering") both the growing oxide and the oxidation tube of sodium ion contamination (Ref 17:94). Additionally, the use of a chlorine additive exhibits a passivation of ionic sodium (in the oxide) introduced as a surface contaminant during metallization or other processing steps disjoint from actual oxidation. This passivation phenomenon is due to the fact that an oxide grown in the presence of HCl incorporates chlorine within the oxide, and subsequently sodium ions are "trapped" by combining with chlorine atoms (Ref 18:363). This same technique also exhibits the advantage of suppressing stacking faults arising during oxide growth at high temperatures. This advantage is more applicable to MOS than p-n junction devices, however, it still results in a more reliable oxide diffusion mask by reducing the possibility of the dopant impurities diffusing rapidly along a crystalline line defect through the oxide layer (Ref 19, 20).

Backside Gettering. Another method of reducing the leakage current arising from mobile ionic impurities is a technique known as backside gettering. This technique

basically involves the creation of crystal lattice defects on the surface of the backside or substrate of the silicon wafer. This is accomplished by roughing up the bottom surface of the wafer using coarse sandpaper or emery cloth. The gettering effect is due to the fact that mobile contaminant ions become immobilized in the lattice defects which act as trap sites. This technique relies on the premise that the highly mobile ionic impurities diffuse much more rapidly through the silicon crystal lattice than do the dopant impurities. Use of this technique can increase yield by as much as 30 percent (Ref 21).

Preliminary Processing Considerations

The oxidation processes mentioned in this thesis all involved a dry/wet/dry growth cycle, with most of the oxide growth occurring during the wet (oxygen + steam) phase of the process. This scheme was employed because it offered the following advantages: (1) Faster growth rate than obtainable by exclusively wet growth because the rapid initial growth rate of dry oxide on bare silicon is taken advantage of, (2) dense dry oxide reduces undercutting at the end of an oxide etch resulting in more sharply defined patterns, (3) dense dry oxide sill have less crystal defects providing a better base for subsequent wet oxide, and (4) rapid wet oxide growth reduces time needed to grow required oxide thickness during critical diffusion drives. HCl gettering was employed during the wet cycle of oxide growth by

using a 6 percent HCl and 94 percent deionized water solution as the liquid in the quartz tank of the steam bubbler.

The next step was to evaluate the processing time and temperatures of Ballantine's processing schedule for the critical gate junction depth. This is documented in the next chapter.

III. Calculations for Fabrication

Introduction

Before actual device processing could commence, it was necessary to determine exactly what Ballantine's processing schedule had produced. Since the gate diffusion is the processing step which determines the most critical of the JFET device parameters, all diffusion times and temperatures affecting the gate junction depth had to be carefully verified. Total reliance upon numerical results obtained solely from complementary error function and gaussian models of the concentration profile were deemed to be too inaccurate for the precision required of the gate junction placement for several reasons.

The first reason for this computational inadequacy is that the diffusion coefficient is extremely difficult to determine by theoretically based calculations. Ballantine experienced great difficulty in determining acceptable values for diffusion coefficients applicable to the temperatures set forth in his processing schedule. The great difficulty of arriving at a valid diffusion coefficient stems from the fact that several interacting parameters directly affect its value, i.e. type of impurity dopant, type of background material being diffused into and its crystal orientation, concentration of impurity dopant, background concentration, and temperature. Additionally, the concentration parameters are not necessarily constant during

the duration of the diffusion. The calculations necessary to correctly determine the diffusion coefficient are quite involved, to say the least, and even when they are accurately performed, there is still no guarantee that theory will correctly approximate what is experimentally observed in the laboratory.

In view of these considerations, the most expedient and accurate method of determining a usable value for the diffusion coefficient of boron at the selected processing temperatures would be to perform several trial diffusions at the desired gate diffusion temperature and empirically solve for the diffusion coefficient. The method chosen to accomplish this task was to perform a "simulated" processing run employing diffusion temperatures consistent with Ballantine's processing schedule (see Appendix C). Unpatterned (i.e. no photolithography steps performed) test wafers were used and the junction depths obtained were evaluated by performing a bevel and stain operation after each diffusion step (see Appendix E).

Junction depth data for various deposition and drive times of the diffusions was then used to calculate an empirical diffusion coefficient to be used in formulating a revised processing schedule to be used in this thesis. After the boron diffusion coefficient is empirically determined, the remainder the the chapter contains calculations for the complete processing schedule. Of course, the gate junction depth computation was based upon the empirically

determined diffusion coefficient. Required oxide thicknesses are also computed.

Analysis of Ballantine's Processing Schedule

To test the results of Ballantine's Processing Schedule, three, three-inch wafers were surface cleaned (see Standard Processing Clean of Appendix K) and loaded into the oxidation tube of the diffusion furnace. Since the boat insertion ("push") and withdrawal ("pull") rates used by Ballantine (Ref 6: III, 3-4) were slow enough to avoid warping the wafers due to thermal stress and yet fast enough to allow for a minimum of deviation from the intended time interval at the specified temperature, the same rates would be employed for all diffusion furnace operation of this thesis. Thus, immediately upon being placed into the tube opening, the quartz diffusion boat was pushed into the oxidation tube at the rate of two feet per minute for the first two feet, and then pushed in the remaining two feet in about five seconds to place the wafers at the center of the tube (49.5 inches).

After the initial field oxide of 5000 angstroms had been grown as specified by Ballantine's processing schedule (see Appendix C), the wafers were withdrawn from the tube by pulling the quartz diffusion boat out at the rate of the first two feet in about five seconds, and the last two feet at the two feet per minute rate. At this point it should be noted that the times to push and pull the wafers are in-

cluded in the total processing time. This is true of all processing phases henceforth.

After the oxide growth cycle, the oxide thickness of each wafer was measured with an ellipsometer. Using the manufacturer's operating instructions (Ref 22, 23), the oxide on wafer DT-1 was determined to be 4780 angstroms, while wafers DT-2 and DT-3 gave thicknesses which measured 4750 angstroms and 4710 angstroms, respectively. Each of these values was within 94 percent of the calculated oxide thickness so processing continued. These oxides were then stripped prior to the subsequent diffusion using undiluted hydrofluoric acid, or HF. A bevel and stain was then performed (see Appendix E) to measure the thickness of the epitaxial layer (epi). The epi thickness after the 5000 angstrom oxide had been stripped was measured to be approximately 1.8 microns for each of the three wafers using a microscope with an interferometer attachment.

After a standard clean had been performed, the wafers were once again loaded into the oxide tube for a "mock" isolation diffusion to determine how deep the epitaxial layer would diffuse. No boron doping was accomplished in order that the epitaxial layer could be distinguished after bevelling and staining, and so that a bevel and stain after the subsequent gate diffusion would reveal the junction depth of the gate region. Had an actual isolation diffusion using the boron sources been performed, the epi would be indistinguishable from the substrate. Since the isolation

diffusion goes completely through the epi, the entire layer would stain dark (since it is now doped p-type) and thus match the p-type substrate.

After the duration of the specified isolation predeposition and drive steps, i.e. 440 minutes (See Appendix C), the test wafers were removed from the furnace tube. A bevel and stain revealed the thickness of the epitaxial layer to be approximately 2.2 microns. This indicated the epi junction had diffused an additional 0.4 microns during the isolation diffusion. This value differs from the 0.5450 micron value expected by Ballantine (Ref 6: III, 25) by about 27 percent.

A surface clean (see Appendix K) was again performed on the test wafers which were then loaded into a quartz diffusion boat with the boron diffusion sources and pushed to the center of the p-tube for a 15 minute gate predeposition (predep). The boat was then removed from the furnace and the borosilicate glass which formed during the predep was removed using cleaning/etching solution CL2 (see Appendix B). The surface resistivity of each wafer was measured with a four-point probe according to the manufacturer's operating instructions (Ref 24). Each wafer was probed in 5 different locations, and the average surface resistivity was then calculated and recorded in Table III-1. The values agreed with those specified by the PDS manufacturer (Ref 25) as well as with the values obtained by Ballantine (Ref 6). A small piece of each wafer (approximately 8 mm from the wafer edge)

was broken off using a diamond tipped scribe and a bevel and stain was performed. The interferometer indicated that the boron had diffused approximately 0.5 micron. This value is consistent with the 0.4939 micron value predicted by Ballantine (Ref 6: III, 27).

The test wafers were once again surface cleaned and placed in the p-tube of the diffusion furnace, without the source wafers, to accomplish the gate drive (see Appendix C). After the drive, a four-point probe was performed on the wafers, and the average surface resistivity was once again determined and listed in Table III-1. The values obtained were once again in agreement with those obtained by Ballantine (Ref 6: III, 13).

Table III-1. Average Boron Surface Resistivity (R_S in ohms/square)

Wafer Identification:	DT-1	DT-2	DT-3
Prior to Predep.--	4300	4250	4400
After Predep.-----	12.5	13.0	13.1
After Drive -----	18.5	19.6	19.8

A bevel and stain was again performed on a chip from the edge of each test wafer. This time the edge of the epi layer was not discernible. The entire bevelled edge had stained dark, indicating that the p-type region had diffused completely through the epi and into the substrate after the gate drive. Evidently, Ballantine's gate diffusion time was much too long. The next course of action was to attempt to

empirically determine the diffusion coefficient through numerous diffusion trials of varying time intervals. This diffusion coefficient would then be used in subsequent calculations for the revision of Ballantine's processing schedule. In order to salvage as much of the original schedule as possible, it was decided to retain the 1050° C temperature for the gate diffusion.

Diffusion Trials

Since the junction depth of the source/drain diffusion was not a critical device parameter of the JFETs to be fabricated, junction depth data for phosphorous diffusion was not collected and the results obtained by Ballantine concerning the phosphorous source/drain diffusion (Ref 6: III, 28) were used when required. Only data pertinent to the diffusion of boron was concentrated upon. Thus, in an effort to empirically determine the value of the boron diffusion coefficient, several boron diffusions of varying time intervals were performed. Bevel and stain operations were performed to evaluate the various junction depths.

Numerous trials were performed before a set of data were arrived at in which any degree of confidence could be placed due to the fact that the initial results were inconsistent. Therefore, only the last segment of data which afforded a high degree of confidence will be presented in this chapter. The initial lack of consistency was due to a three part stain (Ref 26: III, N, 39) of HNO_3, HF, and HAc

in a ratio of 3:1:10. This stain was later discovered to be a silicon etchant when used in a slightly different mixture ratio, the etch rate of which ranges from 76 microns per minute to 100 microns per minute, depending upon the relative concentrations of the three constituent chemicals (Ref 26: III, M, 15).

Evidently, depending upon the length of time taken to stain the sample, an indeterminable but significant amount of the silicon surface had been etched away, thus producing inconsistencies among the various junction depths measured. Upon realization of this fact, the use of this parasitic stain was discontinued and a 10:1 HF stain (see Appendix D) was subsequently utilized. In instances where this stain mix failed to produce results within 5 to 10 minutes, an undiluted HF solution was used. The straight HF usually stained the p-type regions dark within several seconds.

The gate diffusion trials were performed in a similar manner to that of the previous run using Ballantine's processing schedule. One test wafer, scribed and broken into four equal quarters was used, and no photolithography steps were performed. The wafer used was from Microwave Associates Inc., 2 microns n-type epi, with a resistivity of 0.9 ohm-cm. The 20 mils p-type (100) substrate had a resistivity of 40 ohm-cm. Since it was a rejected control wafer (by the manufacturer) from the same lot of wafers to be used later for actual circuit fabrication, the results obtained should be directly applicable to actual device processing.

A 4000 angstrom field oxide was grown (as opposed to 5000 Å) since it was determined that this oxide thickness should be adequate to mask the subsequently shortened diffusion times. The initial boron isolation diffusion is the limiting factor and 4000 angstroms should be more than sufficient for the total of 600 minutes at 1050° C that boron diffuses during (Ref 17: 142). As before, the isolation diffusion was carried out with no Boron Dopant Sources present to allow for diffusion of the epi without counterdoping the entire n-type layer to p-type. The results of these diffusion trials are summarized in Table III-2 and Table III-3. The photographs of interferometer measurements from bevel and stain operations used to compile these two tables are included in Appendix F.

Phosphorous Test Diffusions

Prior to actual device processing, the phosphorous dopant sources had to be checked to ensure they functioned properly. Since junction depth was not a critical parameter (as previously mentioned) the only matter of concern was the

Table III-2. Diffusion of Epitaxial Layer

Condition	Layer Thickness		Distance Diffused
Original Epi (Prior to Initial Oxidation)	8.0 fringes->	2.16 μm	0.000 μm
After 4000A Stripped (20-40-20, 80 minute total oxide growth cycle @ 1050° C)	7.3 fringes->	1.971 μm	-0.189 μm
After 440 minute Isolation Diffusion (26400 sec. @ 1050° C)	9.0 fringes->	2.430 μm	0.459 μm

One fringe line (interference pair) = 0.27 microns
($\lambda/2$ = 2700 A)

concentration of impurity atoms doped into the source and drain regions to enhance the n-type region to that of n+. In order that good ohmic contact be established between the diffused region and the metal contacts, it is desired that the surface concentration be at least 10^{19} cm^{-3} (Ref 27: 349) to overcome the Schottkey barrier effect.

This concentration equates to a resistivity of 0.0064 ohm-cm (Ref 28: 76) or R_s= 30 ohms/square (at most) surface resistance assuming a 2 micron junction depth as the worst case boundary condition. Thus the only constraint on the phosphorous enhancement diffusion was that the surface resistance be no greater than 30 ohms per square (assuming undiffused virgin silicon) after the final diffusion drive has been accomplished.

Table III-3. Diffusion of Boron At 1050° C

Condition	Junction Depth	Distance Diffused
12 minute Predep (720 seconds)	1.2 fringes-> 0.324 µm	0.324 µm
12 minute Predep + 30 minute Drive (2520 seconds)	2.7 fringes-> 0.729 µm	0.729 µm
12 minute Predep + 40 minute Drive (3120 seconds)	4.3 fringes-> 1.161 µm	1.161 µm
12 minute Predep + 30 minute Drive + 15 minute Phosphorous Predep @ 1000° C (3420 seconds)	4.4 fringes-> 1.188 µm	1.188 µm
15 minute Predep (900 seconds)	1.8 fringes-> 0.486 µm	0.486 µm
15 minute Predep + 30 minute Drive (2700 seconds)	4.4 fringes-> 1.188 µm	1.188 µm
15 minute Predep + 40 minute Drive (3300 seconds)	5.0 fringes-> 1.350 µm	1.350 µm
15 minute Predep + 30 minute Drive + 15 minute Phosphorous Predep @ 1000° C (3600 seconds)	5.2 fringes-> 1.404 µm	1.404 µm

One fringe line (interference pair) = 0.27 microns
($\lambda/2$ = 2700 A)

To accomplish the phosphorous diffusion test, two, three-inch test wafers were surface cleaned and pushed to the center of the n-type diffusion tube along with the phosphorous dopant sources. The specified predep was for 15 minutes at 1000 degrees C. The phosphorous source wafers used were: Planar Diffusion Sources, Phosphorous, Grade PH-1000 manufactured by PDS, Graphite Products Division, Carborundum Co. The silicon wafers used were some of the same wafers used for the boron test diffusions.

After the predep, a four-point probe indicated that the surface resistance was essentially unchanged from the values which existed prior to the phosphorous predep as a result of the previous boron drive. To further investigate why the phosphorous wafers were not functioning properly, test wafers were placed adjacent to existing source wafers in positions differing from those previously used. The phosphorous wafers still produced very little alteration of the surface resistance for the silicon test wafers after the 15 minute predep.

At this point, believing the source wafers to be defective, brand new phosphorous source wafers were placed in the quartz diffusion boat. The source wafers were then placed in the p-type diffusion tube and were slowly pushed to the center of the tube over the course of 5 minutes to avoid stressing the wafer due to thermal shock. The wafers remained in the hot zone for 30 minutes to activate the sources as specified by the manufacturer (Ref 28). The boat

was then slowly withdrawn from the tube and two undiffused test wafers were loaded into the boat which was again placed in the center of the tube for 15 minutes.

A subsequent four-point probe revealed the surface resistivity to be 55 ohms/square for one wafer and 99 ohms/square for the other. These values were still not low enough and did not agree with the data supplied by the manufacturer (Ref 28). The decision was then made to increase the temperature of the tube from 1000° C to 1025° C to remedy the low doping concentration problem. At this point it was discovered that the n-type diffusion tube was at a temperature 150° C lower than it was believed to be.

This misprofiling of the phosphorous tube caused the most significant loss of time spent on this thesis. The tube was re-profiled to 1000° C (See Appendix A) and a diffusion test was performed once again. The wafers used for the initial phosphorous diffusion test were: Microwave Associates Inc., 3.8-4.2 microns n-type epi with a resistivity of one ohm-cm, on a p-type substrate. This time satisfactory results were obtained. The four-point probe resulted in values consistent with those achieved by Ballantine (Ref 6: III, 35) as well as with the data supplied by the manufacturer (Ref 28). The test results are tabulated in Table III-4.

Table III-4. Average Phosphorous Surface Resistivity (R_s in ohms/square)

Wafer Identification:	PD-1	PD-2
Prior to Predep.--	1520	1490
After Predep.-----	14.3	13.8
After Drive -----	11.5	10.9

15 minute Predep & 20 minute Drive at 1000° C

Determination of Diffusion Coefficients

The diffusion process is dominated by four parameters: time, temperature, impurity doping concentration gradient, and type of impurity. The type of impurity influences the diffusion rate through a parameter known as its diffusion coefficient, D. The greater the value of D, the more rapidly it diffuses for a given temperature and concentration gradient.

Epitaxial Diffusion Coefficient. The following equation can be used to model the diffusion of the epitaxial layer (epi) during processing (Ref 8: 80):

$$N(x,t) = \frac{1}{2} N_{epi} \operatorname{erfc}\left(\frac{x_j}{2\sqrt{Dt}}\right) \qquad \text{(III-1)}$$

where

$N(x,t)$ is the impurity concentration as a function of time and diffused length,

N_{epi} is the bulk impurity concentration of the epi,

x_j is the junction depth at which $N(x,t)$ equals N_B, the bulk or background concentration,

Dt is the diffusion coefficient, time product, and erfc denotes the complimentary error function.

Since the epi is specified according to the manufacturer as 2 microns thick with a resistivity of 0.9 ohm-cm, the impurity concentration of the epi is determined to be $6x10^{15}$ cm^{-3} (Ref 8: 113). The impurity concentration of the substrate is specified as $5x10^{14}$ cm^{-3} by the manufacturer. This value is N_B since the substrate becomes the background into which the epi diffuses. Since the epi is uniformly doped and two microns thick, it can be assumed to be an infinite impurity source for which case the erfc model is applicable (Ref 8: 67).

After solving Eq (III-1) for the erfc and substituting for the constant values, the following equation for epi junction depth as a function of diffusion coefficient and time is obtained:

$$x_j = 1.9560\ (Dt)^{1/2} \qquad \text{(III-2)}$$

Using the values of $x_j = 0.459x10^{-4}$ cm and $t = 26400$ seconds (from Table III-2), the effective diffusion coefficient governing diffusion of the epi is determined to be $2.0859x10^{-14}$ cm^2-sec^{-1} at 1050° C. This value is 14 percent less than what Ballantine had estimated it to be (Ref 6: III, 25). This empirically derived diffusion coefficient for epi diffusion closely supported the subsequent data observed in the laboratory.

Boron Diffusion Coefficient. The equation which approximates the concentration profile for a constant source diffusion is given as (Ref 8: 49)

$$N(x,t) = N_o \text{ erfc}\left(\frac{x_j}{2\sqrt{Dt}}\right) \qquad \text{(III-3)}$$

where N_0 is the solid solubility limit of the impurity at the temperature at which the diffusion takes place. For the case of the data listed in Table III-3, $N_o = 4x10^{20}cm^{-3}$ for boron in silicon at 1050 degrees C (Ref 29: 241). Additionally, $N_B = 6x10^{15}cm^{-3}$ since boron is diffusing into the epi, and the epi is therefore the background.

Solving for the erfc and the x_j in Eq (III-3), and substituting for N_B and N_o yields Eq (III-4):

$$x_j = 6.1218\ (Dt)^{1/2} \qquad \text{(III-4)}$$

for a constant source diffusion into silicon, e.g. predep. Using the data of Table III-3 and Eq (III-4), the diffusion coefficient for boron in silicon at 1050 degrees C is determined to be $D = 7.0028x10^{-14}cm^2\text{-}sec^{-1}$. Under the assumption that the ratio of the diffusion coefficient at 1050° C to that at 1000° C as determined by Ballantine is valid, the boron diffusion coefficient at 1000°C is 30 percent of the value for 1050°C (Ref 6: II, 4). For the purpose of calculations a value of $D = 2.1008x10^{-14}\ cm^2\text{-}sec^{-1}$ will be used for diffusion times at 1000 degrees C.

Phosphorous Diffusion Coefficient. The junction depth of the enhancement diffusion for the source and drain regions is not critical, as mentioned previously. Therefore, the value of $D = 2.0175 \times 10^{-13} cm^2\text{-}sec^{-1}$ (Ref 6: 23-28) is assumed to be accurate enough for the purpose of subsequent calculations at 1000°C.

Initial JFET Fabrication Calculations

The initial processing schedule of Appendix I was developed using Ballantine's processing schedule (Ref 6: F, 1) as a rough framework. This processing schedule was arrived at after drawing conclusions from the diffusion trials summarized in Tables III-2 and III-3.

The critical JFET parameter yet to be resolved is the width of the channel below the gate region. It is desired that each JFET of the array have a pinch-off voltage of -3 V to facilitate the use of the existing NMOS multiplexer chip (Ref 6: V). The parameter which governs this value is the width of the depletion regions formed in the n-channel below the gate due to the reverse biased gate junction and the built-in pn junction potential where the epi and substrate meet (see Figure III-1). In order to pinch-off the n-type

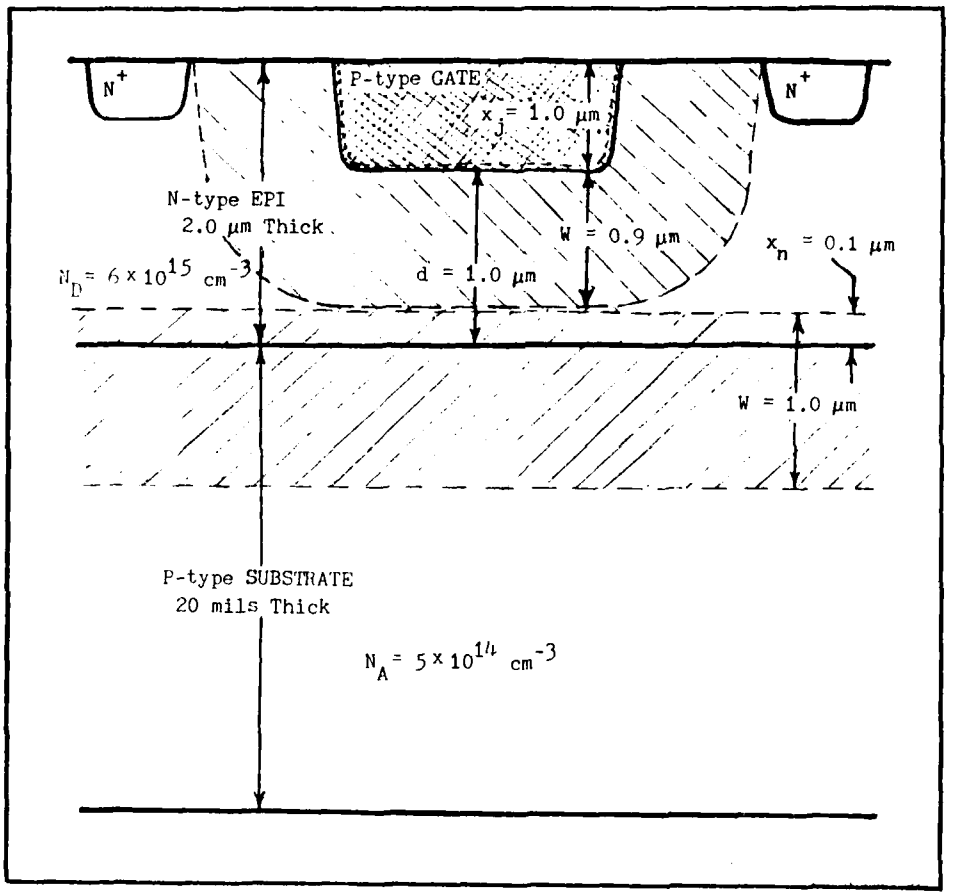


Figure III-1. Depletion Regions Relative to N-channel

conduction channel between the source and drain, the channel width, d, must be less than or equal to the sum of the width of the space charge depletion region (SCDR) at the reverse biased gate junction and the SCDR due to the built-in pn junction potential at the epi/substrate junction.

The width of the SCDR at the substrate extending into the epi can be determined as follows. The total depletion region width W of a step junction as a function of total electrostatic potential from one side of the junction to the other ϕ_B is given as (Ref 8: 159)

$$W = \sqrt{\frac{2K_s \epsilon_o}{q} \frac{N_A + N_D}{N_A N_D} \phi_B} \qquad \text{(III-5)}$$

where K_s= 11.7 is the dielectric constant for silicon,

$q = 1.60 \times 10^{-19}$C is the magnitude of electronic charge,

$N_A = 5 \times 10^{14} cm^{-3}$ is the acceptor concentration of the P-type region (substrate), and

$N_D = 6 \times 10^{15} cm^{-3}$ is the donor concentration of the n-type region (epi channel).

The junction potential is determined by (Ref 8: 157)

$$\phi_B = \phi_{Fp} + |\phi_{Fn}| \qquad \text{(III-6)}$$

where ϕ_{Fp} and ϕ_{Fn} are the Fermi potentials on the p and n sides of the junction, respectively as given by (Ref 8: 157):

$$\phi_{Fp} = \frac{kT}{q} \ln \frac{N_A}{n_i} \qquad \text{(III-7)}$$

$$\phi_{Fn} = -\frac{kT}{q} \ln \frac{N_A}{n_i} \qquad \text{(III-8)}$$

where

$\frac{kT}{q} = 0.026$ V is the Boltzmann, temperature product at T = 300 degrees C, and

$n_i = 2.5 \times 10^{13} cm^{-3}$ is the intrinsic carrier concentration of silicon at 300 degrees C (Ref 30: 51).

After substituting values into Eq (III-5), the total depletion region width is found to be

$$W = 1.02 \times 10^{-4} cm \text{ or } 1.02 \text{ microns}$$

Since only the width of the SCDR in the epi is of interest, the portion of W on the n-side of the junction, x_n, must be determined using the following equation (Ref 8: 158)

$$x_n = \frac{N_A}{N_A + N_D} W \qquad \text{(III-9)}$$

which yields a value of $x_n = 0.08 \times 10^{-4} cm$ or approximately 0.1 micron. The SCDR width associated with the gate junction can similarly be calculated using (Ref 8: 248)

$$W = \sqrt{\frac{2K_s \epsilon_o (\phi_B + V_G)}{qN_D}} \qquad \text{(III-10)}$$

where $V_G = -3$ V is the gate voltage (at pinch-off), and

$\phi_B \approx 0.7$ V is the built-in pn junction potential.

Solving Eq (III-10) yields $W = 0.893 \times 10^{-4} cm$ or approximately 0.9 microns. Thus the target value for the channel width,

d, is the sum of these depletion widths or d = 1 micron.

In order to achieve the desired minimum channel width of 1 micron, the gate junction must diffuse approximately 1 micron into the epi. Ballantine's processing schedule (Ref 6: F, 1) clearly could not satisfy this constraint, and consequently it was revised as listed in Appendix I to remedy this failing. Major changes involved reducing the field oxide from 5000 Å to 4000 Å and shortening the gate predep and drive times as well as shortening the phosphorous source/drain drive. The field oxide was reduced in order to save approximately 0.05 microns of epi otherwise consumed in excess oxide growth. It was not decreased further for fear that it may be too thin to withstand the numerous cleans involving HF.

The limiting factor for the minimum length of the gate and source/drain drive times was the time required to grow an adequate thickness of oxide to mask the subsequent diffusion and form an adequate insulating layer prior to metallization. Approximately 3000 Å of oxide is necessary to mask the 25 minute source/drain diffusion (Ref 17: 142) for phosphorous at 1000°C, and it is desired that there be at least 1000 Å of oxide covering the source and drain diffusions prior to metallization.

Oxide growth times were arrived at using time/thickness growth curves (Ref 17: 92, 93). Since these curves produced satisfactory results during the oxidation steps of Chapter II, no other thickness tests to validate oxide growth cycle

times were performed prior to processing. The oxide thicknesses were checked using an ellipsometer at intermediate steps during processing. Additionally, Ballantine's cycle times were available for the various desired oxide thicknesses for identical processing temperatures.

Estimation of Diffusion Profiles

In order to formulate a complete processing schedule, it was first necessary to mathematically approximate where the device junctions will be upon completion of processing. The calculations themselves are straight forward, however, most of the high temperature processes are interdependent. This fact causes difficulty because changing one process affects other processes, and therefore the calculations for each affected process also change.

Due to the interdependency of the calculations for the diffusion of the epi, isolation, gate, and enhancement regions, several iterations of the calculations which ensue were performed before the final set of predicted junction depths and cycle times were determined. Only the final set of calculations which are applicable to the initial processing schedule are shown.

Since two step diffusions were to be implemented for each impurity doping operation, it was necessary to perform separate calculations to predict junction depths for the predeposition step and for the drive or oxidation step. The diffusion drive is not a constant source diffusion as with

the predep, and therefore cannot be approximated by the erfc concentration profile of Eq (III-3). The source wafers could not be present during drive step, because the steam ambient would ruin the planar diffusion source during oxidation. The drive step was therefore a "limited source" diffusion and the impurity atoms assume a Gaussian distribution as opposed to the erfc concentration profile of a "constant source" diffusion employed for the predep.

The Gaussian concentration profile resulting from diffusion drives is described by the following equation (Ref Ref 8: 50):

$$N(x,t) = Q(Dt)^{-1/2} \exp[-x_j^2 (Dt)^{-1}] \qquad \text{(III-11)}$$

where Q is the number of atoms deposited during the predep, as given by the following equation:

$$Q = 2N_o(Dt)^{1/2} \pi^{-1/2} \qquad \text{(III-12)}$$

Using Eqs (III-2), (III-4), (III-11), and (III-12), the diffusion of each layer was analyzed individually in the discussion which follows in order to support a revision of Ballantine's processing schedule, starting with the prediction of epi junction depth.

Epitaxial Layer Diffusion. The diffusion of the epi into the substrate progresses at an extremely slow rate since the concentration gradient between the epi layer and the substrate is rather small. Since difficulty exists in

obtaining the required one micron channel width between the gate junction and the epi/substrate junction, it is desirable to widen the epi layer as much as possible by taking full advantage of its drift into the substrate.

To maximize this drift, a liberal amount of growth time for the initial field oxide was employed by utilizing lengthy dry oxidation intervals for the initial growth cycle and anneal cycle to prolong the time required to grow the desired oxide thickness and placing less reliance on the rapid growth of the short, wet oxidation interval.

Eq (III-2) was used to compute the epi layer diffused depth at the end of each process. Table III-5 summarizes the results of these calculations.

Isolation Diffusion. The isolation diffusion consists of a boron predeposition (predep) and an initial drive. Additionally, all drives of subsequent processes also contribute to the time during which the isolation region diffuses. The predep and drive times for the isolation diffusion were selected such that the boron region would dif-

Table III-5. Initial Calculations for Epi Diffusion

Processing Step	t (sec)	Dt (cm^2)	ΣDt(cm^2)	x_j(μm)
Initial Oxide 90 min. @ 1050° C	5400	1.1264×10^{-10}	1.1264×10^{-10}	0.2076
Isolation Predep 40 min. @ 1050° C	2400	5.0062×10^{-11}	1.6270×10^{-10}	0.2495
Isolation Drive 400 min. @ 1050° C	24000	5.0062×10^{-9}	6.6332×10^{-10}	0.5038
Gate Predep 12 min. @ 1050° C	720	1.5018×10^{-11}	6.7834×10^{-10}	0.5094
Gate Drive 30 min. @ 1050° C	1800	3.7546×10^{-11}	7.1589×10^{-10}	0.5233
Source/Drain Predep 15 min. @ 1000° C	900	5.6319×10^{-12}	7.2152×10^{-10}	0.5254
Source/Drain Drive 15 min. @ 1000° C	900	5.6319×10^{-12}	7.2715×10^{-10}	0.5274

$$N(x,t) = N_S(0.5)(\text{erfc}(x_j(.05)(Dt)^{-1/2})) \rightarrow x_j = 1.9560(Dt)^{1/2}$$

$$D = 2.0859 \times 10^{-14}\ cm^2\text{-}sec^{-1} \text{ at } 1050°\ C$$

$$D = 6.2577 \times 10^{-15}\ cm^2\text{-}sec^{-1} \text{ at } 1000°\ C$$

$$N_S = C_{epi} = 6 \times 10^{15}\ cm^{-3}$$

$$N_B = C_{substr} = 5 \times 10^{14}\ cm^{-3}$$

fuse completely through the epi and into the substrate, thus forming an isolation well around each JFET to isolate them from each other.

The time duration of this diffusion was chosen to be as long as possible to once again take advantage of epi drift to maximize the channel width. The limiting factor on the maximum time was set by two considerations. First, the drive time must be short enough to avoid excessive lateral diffusion of the isolation region, and secondly, it must not be so long that the transition from epi to substrate be degraded sufficiently to invalidate a step junction approximation.

Eqs (III-4), (III-11), and (III-12) were used to compute the diffused depth of the isolation region. First, the junction depth after the predep was calculated using Eq (III-4). Then the number of atoms deposited during the predep was calculated using Eq (III-12). The diffused depth after each processing step was then computed using Eq (III-11) for the sum of the drive times at the applicable temperature. Since the distance diffused during the predep is significant, it was necessary to add this previously calculated depth to the diffused distance during the drive time.

The results of these calculations are shown in Table III-6. It was assumed that the impurity doping concentration produced by the predep at the surface was equal to the solid solubility of the impurity at the temperature at which it was deposited.

Table III-6. Initial Calculations for Isolation Diffusion

Processing Step	t (sec)	Σt (sec)	ΣDt(cm^2)	x_j(μm)
Isolation Predep 40 min. @ 1050° C	2400	2400	1.6807×10^{-10}	0.7936
Isolation Drive 400 min. @ 1050' C	24000	24000	1.6807×10^{-9}	3.3214
Gate Predep 12 min. @ 1050° C	720	24720	1.7311×10^{-9}	3.3570
Gate Drive 30 min. @ 1050° C	1800	26520	1.8571×10^{-9}	3.4438
Source/Drain Predep 15 min. @ 1000° C	900	27420	1.8760×10^{-9}	3.4564
Source/Drain Drive 15 min. @ 1000° C	900	28320	1.8949×10^{-9}	3.4692

$$N(x,t) = N_o(\text{erfc}(x_j(.05)(Dt)^{-1/2})) \rightarrow x_j = 6.1218(Dt)^{1/2}$$

$$Q(t) = 2N_o(Dt)^{1/2}\,\pi^{-1/2} = 5.8514 \times 10^{15}\ cm^{-2}$$

$$N(x,t) = Q(Dt)^{-1/2}(\exp(-x_j^2(Dt)^{-1}))$$

$$N_o = 4 \times 10^{20}\ cm^{-3}$$

$$N_B = 6 \times 10^{15}\ cm^{-3} = C_{epi}$$

$$D = 7.0028 \times 10^{-14}\ cm^2\text{-}sec^{-1} \text{ at } 1050°\ C$$

$$D = 2.1008 \times 10^{-14}\ cm^2\text{-}sec^{-1} \text{ at } 1000°\ C$$

Gate Diffusion. The gate diffusion is similar to the isolation diffusion being that it consists of a boron predep, initial drive, and subsequent drives at 1050 degrees C

and 1000 degrees C into the epitaxial layer. The major difference is that Q(t) is not as great as it was for the isolation diffusion, since the gate predep time was much smaller than that which was used for the isolation diffusion. The same equations used for the isolation computations were used to calculate the gate diffusion depth after each processing step (see Table III-7).

Source/Drain Diffusion. The source/drain diffusion is the last high temperature process and consists of a phosphorous predep and drive at 1000 degrees C into the epi. During the predep, phosphorous source wafers are used to affect a solid solubility limit of $1x10^{21}cm^{-3}$ (Ref 29: 241). The diffusion coefficient for phosphorous, at 1000 degrees C and at the above impurity doping concentration, is assumed to be $2.0175x10^{-13}$ cm^2-sec^{-1} (REf 8: 39). Using Eqs (III-3), (III-11), and (III-12) again to compute the diffused depths at 1000 degrees C, the information of Table III-8 was compiled.

Table III-7. Initial Calculations for Gate Diffusion

Processing Step	t (sec)	Σt (sec)	ΣDt(cm^2)	x_j(um)
Gate Predep 12 min. @ 1050° C	720	720	5.0420×10^{-11}	0.4347
Gate Drive 30 min. @ 1050° C	1800	1800	1.2605×10^{-10}	1.1517
Source/Drain Predep 15 min. @ 1000° C	900	2700	1.4496×10^{-10}	1.2010
Source/Drain Drive 15 min. @ 1000° C	900	3600	1.6386×10^{-10}	1.2470

$$N(x,t) = N_o(\text{erfc}(x_j(.05)(Dt)^{-1/2})) \dashrightarrow x_j = 6.1218(Dt)^{1/2}$$

$$Q(t) = 2N_o(Dt)^{1/2}\,\pi^{-1/2} = 3.2049 \times 10^{15}\ cm^{-2}$$

$$N(x,t) = Q(\,Dt)^{-1/2}(\exp(-x_j^2(Dt)^{-1}))$$

$$N_o = 4 \times 10^{20}\ cm^{-3}$$

$$N_B = 6 \times 10^{15}\ cm^{-3} = C_{epi}$$

$$D = 7.0028 \times 10^{-14}\ cm^2\text{-}sec^{-1} \text{ at } 1050°\ C$$

$$D = 2.1008 \times 10^{-14}\ cm^2\text{-}sec^{-1} \text{ at } 1000°\ C$$

Table III-8. Initial Calculations for Source/Drain Diffusion

Processing Step	t (sec)	Σt (sec)	ΣDt(cm^2)	x_j(um)
Source/Drain Predep 15 min. @ 1000° C	900	900	1.8158×10^{-10}	0.8626
Source/Drain Drive 15 min. @ 1000° C	900	1800	1.8158×10^{-10}	1.7794

$$N(x,t) = N_o(\text{erfc}(x_j(.05)(Dt)^{-1/2})) \dashrightarrow x_j = 6.4015(Dt)^{1/2}$$

$$Q(t) = 2N_o(Dt)^{1/2}\ \pi^{-1/2} = 1.5205 \times 10^{16}\ cm^{-2}$$

$$N(x,t) = Q(\ Dt)^{-1/2}(\exp(-x_j^2(Dt)^{-1}))$$

$$N_o = 1 \times 10^{21}\ cm^{-3}$$

$$N_B = 6 \times 10^{15}\ cm^{-3} = C_{epi}$$

$$D = 2.0175 \times 10^{-13}\ cm^2\text{-}sec^{-1} \text{ at } 1000°\ C$$

Determination of Oxide Mask Thicknesses

Thermally grown silicon dioxide was chosen to serve as the diffusion mask for all processing steps involved. Since the diffusion coefficient for the two dopants (boron and phosphorous) are several orders of magnitude lower in silicon dioxide than in silicon (Ref 29: 210), it should serve to block any diffusion of impurity dopants into the epi other than the regions selected for doping. Additionally, the grown oxide is easily etched through openings in a patterned photoresist layer.

Two oxide mask thicknesses need to be determined. The first is the initial field oxide which must mask all three diffusions, i.e. isolation, gate, and source/drain. The second oxide is grown during the gate drive and is required to serve as a mask for the subsequent source/drain diffusion. It is not critical to mask the isolation region during the gate diffusion because both of these processes use boron as the impurity dopant and there are no ill consequences of enriching a previously doped isolation region during the subsequent gate diffusion.

The initial field oxide must be sufficiently thick to mask boron for a total of 482 minutes at 1050 degrees C, and 30 minutes at 1000 degrees C. To add a margin of safety, the required minimum thickness was determined assuming a temperature of 1050 degrees C for the entire fabrication process, since the diffusion coefficient is greater at the higher temperature. Also, this same oxide must be adequate

to mask phosphorous for 30 minutes at 1000 degrees C.

Approximately 3000 angstroms of oxide is sufficient to mask boron for 600 minutes at 1050 degrees C, and approximately 2500 angstroms of oxide is adequate to mask phosphorous for 30 minutes at 1000 degrees C (Ref 17: 142). An oxide 3000 angstroms thick should therefore be an effective mask for the entire process. To allow a safety margin, however, 4000 angstroms of initial oxide would be grown to make allowance for the reduction of oxide thickness during the numerous cleaning cycles which involve HF.

The second oxide, grown over the isolation and gate diffusions during the gate drive, must be at least 2500 angstroms, as previously discussed, to mask phosphorous during the 30 minute source/drain enhancement diffusion. To allow a margin for error, 3000 angstroms of oxide would be grown during the gate drive.

In addition a third oxide must be grown during the source/drain drive. It serves as a passivation layer and an insulating surface upon which metal contact pads will be placed.

As mentioned in Chapter II, oxide growth will begin in dry O_2 to obtain the rapid initial growth phase, followed by a wet O_2 (steam) cycle during which the oxide is rapidly grown to the desired thickness, and then switching back to dry O_2 to help anneal and densify the oxide. Table III-9 shows the various cycle times required to grow the necessary oxide thicknesses for the processing schedule.

Table III-9. Oxidation Cycle Times for Required Thicknesses

Oxide	Time (minutes)	Temperature (degrees C)	Condition	Thickness (angstroms)
Initial Field Oxide	40	1050	Dry O_2	800
	30	1050	Wet O_2	3200
	20	1050	Dry O_2	negligible
			TOTAL	4000 angstroms
Gate Oxide	3	1050	Dry O_2	100
	25	1050	Wet O_2	2900
	2	1050	Dry O_2	negligible
			TOTAL	3000 angstroms
Source/ Drain Oxide	4	1000	Dry O_2	100
	8	1000	Wet O_2	900
	3	1000	Dry O_2	negligible
			TOTAL	1000 angstroms

Summary of Predicted Junction Depths

From the final junction depths of the diffusion tables compiled previously, and accounting for the amount of silicon consumed due to oxide growth, a cross-section of the wafer is depicted in Figure III-2. This figure shows the expected junction depths of the JFET as predicted by the calculations of this chapter for the processing schedule of Appendix I.

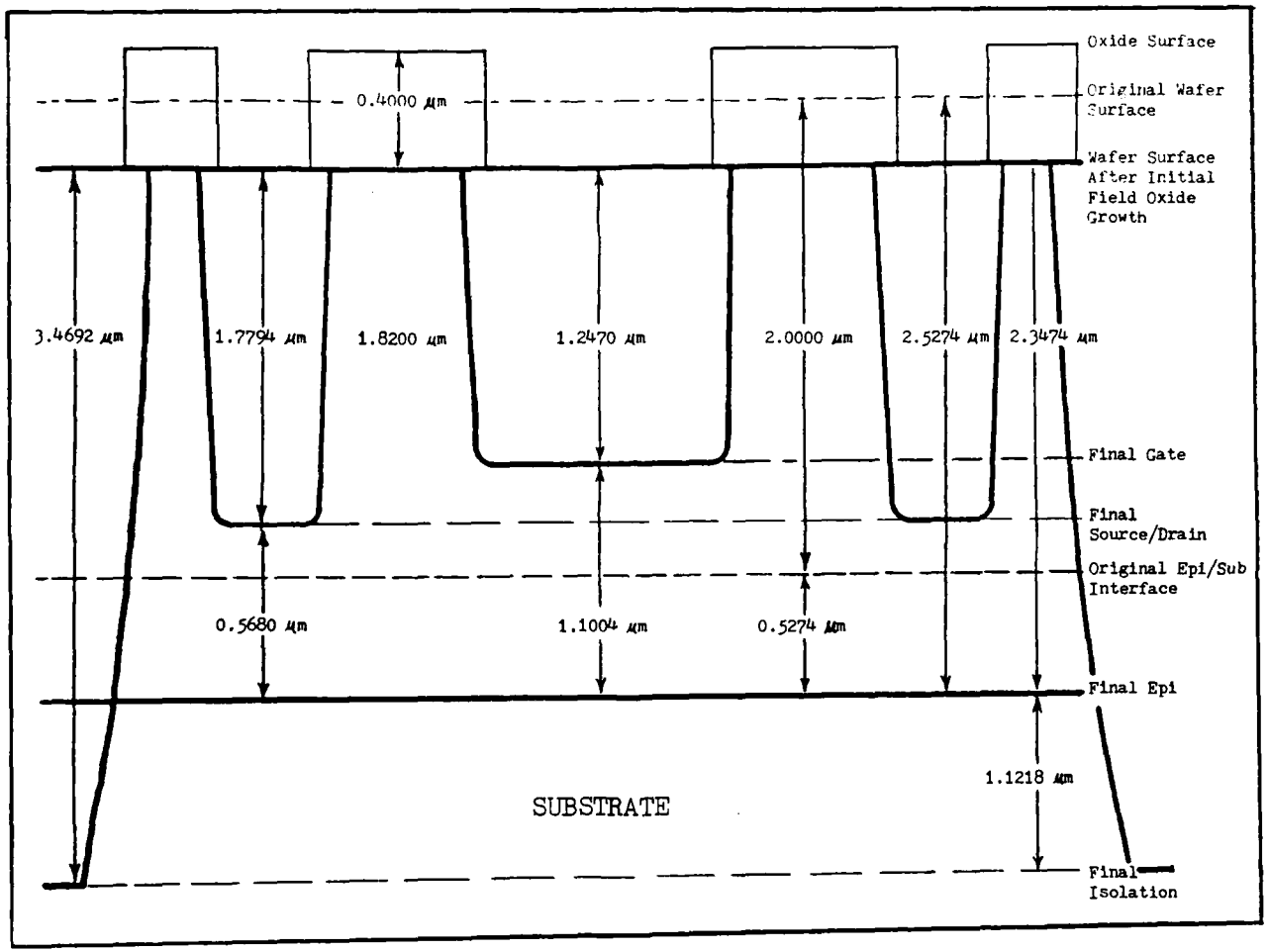


Figure III-2. Pictorial Summary of Estimated Junction Depths

IV. Device Fabrication

Introduction

Since only a limited number (12 to be exact) of three-inch wafers were available for fabrication of the JFET arrays, the most prudent approach to processing was to divide the wafers up into lots to be used in separate, independent fabrication attempts. In this manner, all the wafers would not be ruined as the result of an error in the initial processing schedule or a mishap during processing. The use of independent processing runs also allows for greater flexibility in making mid-course corrections based upon results of prior attempts.

Five independent processing runs were employed; the first four consisted of lots of two device wafers and a half-wafer serving as a control. The final run consisted of three device wafers and one control. This approach offered the highest probability of obtaining working devices. The purpose of the control wafer in each lot was to permit checking the oxide thickness grown and the diffusion depths as the fabrication proceeded and thereby allow for corrections in the diffusion processes as necessary. The initial processing schedule developed in Chapter III and listed in Appendix I was used for the first fabrication run. A cross section of the desired JFET structure is shown Figure IV-1.

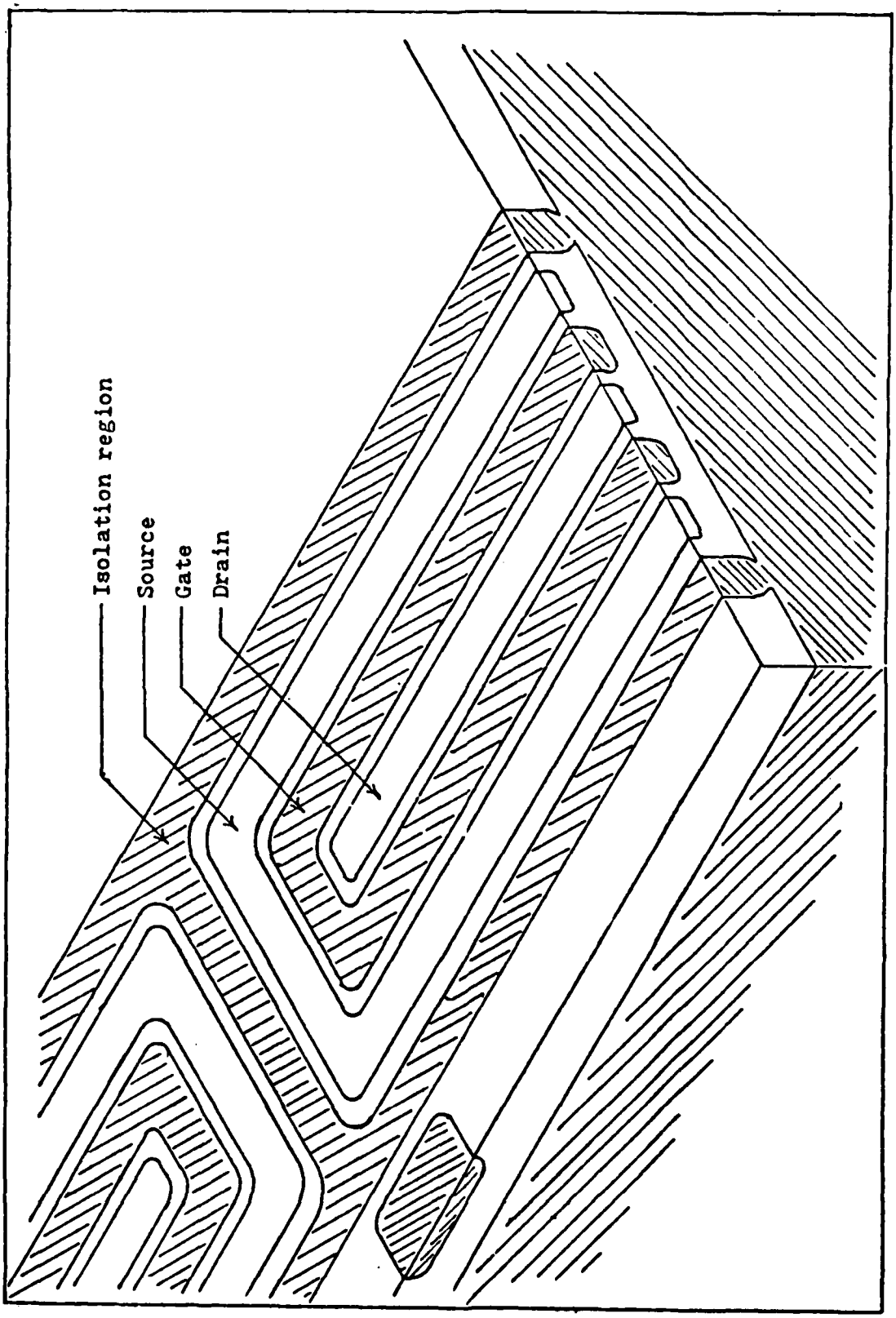


Figure IV-1. Cross Section of Desired JFET Structure (Ref 2)

Details of First Processing Run

Initial Field Oxide Growth. The silicon wafers used for JFET fabrication were: Microwave Associates Inc., 2 microns n-type epi with a 0.9 ohm-cm resistivity on a 20 mil p-type (100) substrate of 40 ohm-cm resistivity. Two and one-half wafers were cleaned using the Standard Processing Clean, loaded into a quartz boat, and then placed in the furnace oxidation tube to grow 4000 angstroms of initial field oxide.

After the oxide growth cycle, each of the three wafers were checked with an ellipsometer to verify the oxide thickness. The thicknesses ranged from 3770 to 3800 angstroms. Although these values were less than the target value of 4000 angstroms, the oxides were still sufficient to mask all the required diffusions and were therefore not placed back in the furnace to grow additional oxide. The next processing step performed was the isolation diffusion.

JFET Isolation Diffusion. The isolation diffusion process consisted of the isolation mask photolithography process, etching of the isolation pattern, and diffusion of the isolation region. The actual isolation diffusion entailed a p-type diffusion of boron that was driven through the n-type epi into the p-type substrate, thus forming an n-type "well" in which each JFET would be made. Isolation was achieved by virtue of the reversed-biased p-n junction surrounding each JFET, thereby isolating each one from the adjacent JFETs.

The photolithography process was initiated by positioning the isolation mask (L1) in the mask aligner which was set up according to the manufacturer's operating instructions (Ref 31). The photolithography steps were performed on the two device wafers as outlined in Appendix G. The mask pattern used is shown in Figure IV-2. Dust did settle on both the mask and wafer during this process, despite the fact that compressed nitrogen was frequently used to blow debris off the surfaces. This caused little visible difficulty due to the fact that lengthy exposure times were involved in conjunction with positive photoresist (PR), which has a dark field. The oxide pattern was then etched using the procedure outlined in Appendix H.

Even if the dust particles were large enough to visibly affect the developed pattern, the result was not catastrophic since positive PR was used. The small area of unexposed PR under the dust speck would result in an "island" being formed in the diffusion window rather a "pinhole" as would result after the etch if negative PR had been used.

After etching, a 40 minute boron predep was performed, followed by a 6 hour and 40 minute drive. The control wafer was not included during the predeposition since the complete p-type doping of the epi during this step would render it useless as a control wafer during the gate diffusion. Note

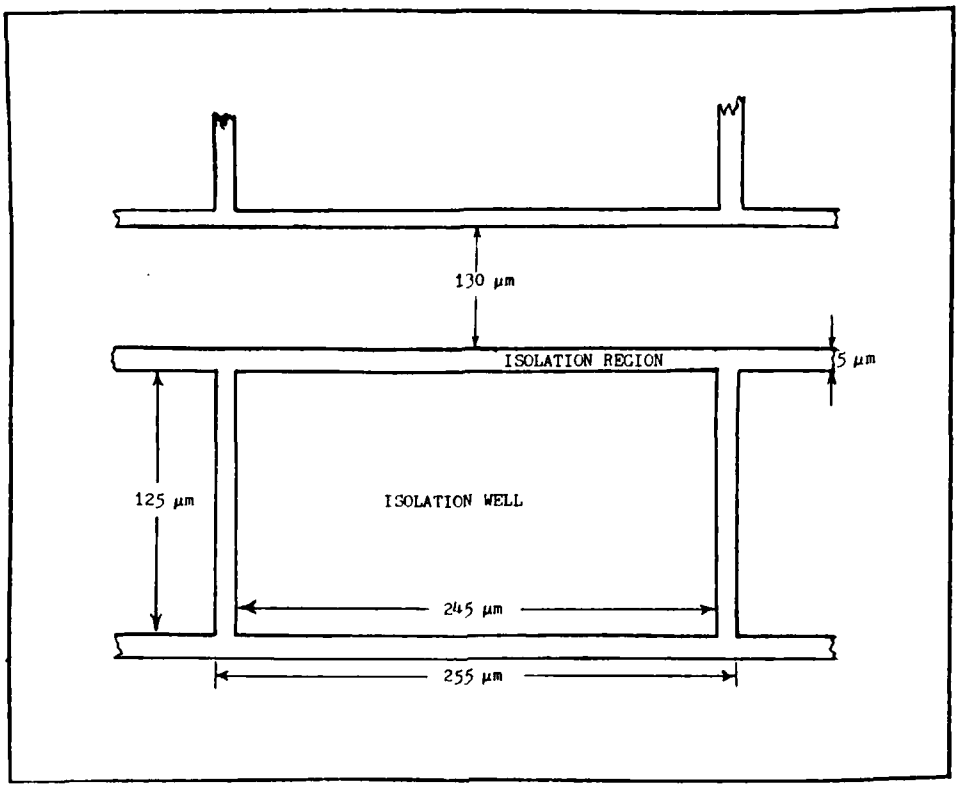


Figure IV-2. Isolation Mask Pattern

that the control wafer was included during the 400 minute drive to affect the same half micron (approximately) of epi junction diffusion as the other wafers. This was done to maintain consistency between the device wafers and the control wafer enabling accurate junction depth evaluation after subsequent processing.

No four-point probe was performed after this diffusion, however a small chip from the edge of a device wafer was examined using a bevel and stain to ensure the boron had indeed diffused completely through the epi and into the substrate. The oxide thickness grown on the control wafer during the drive was measured to be 1910 angstroms. It

should be noted that the oxide grown on the control wafers was always removed prior to each subsequent diffusion.

The same phenomenon of "bubbles" in the isolation windows as experienced by Ballantine (Ref 6: III, 19) were visible under a microscope after completion of the isolation diffusion. This "bubble" anomaly is addressed later in this chapter.

JFET Gate Diffusion. The gate diffusion process was comprised of the gate mask photolithography process, etching of the gate pattern, and the actual gate diffusion. As with the isolation diffusion, the gate diffusion is a p-type diffusion of boron into the epi.

The photolithography process was initiated by positioning the gate mask (L2) in the mask aligner according to the manufacturer's operating instructions (Ref 31), and the photolithography steps were performed on the two device wafers as outlined in Appendix G. The mask pattern is shown in Figure IV-3. After a successful pattern development, the two device wafers were then etched according to the oxide etching procedure listed in Appendix H. Approximately 5.5 minutes were necessary to completely etch the gate pattern clear of oxide. The oxide on the control wafer was completely stripped off using straight HF to etch away the oxide.

After etching the oxide patterns, a 12 minute boron predep was performed. The boron glass was stripped off

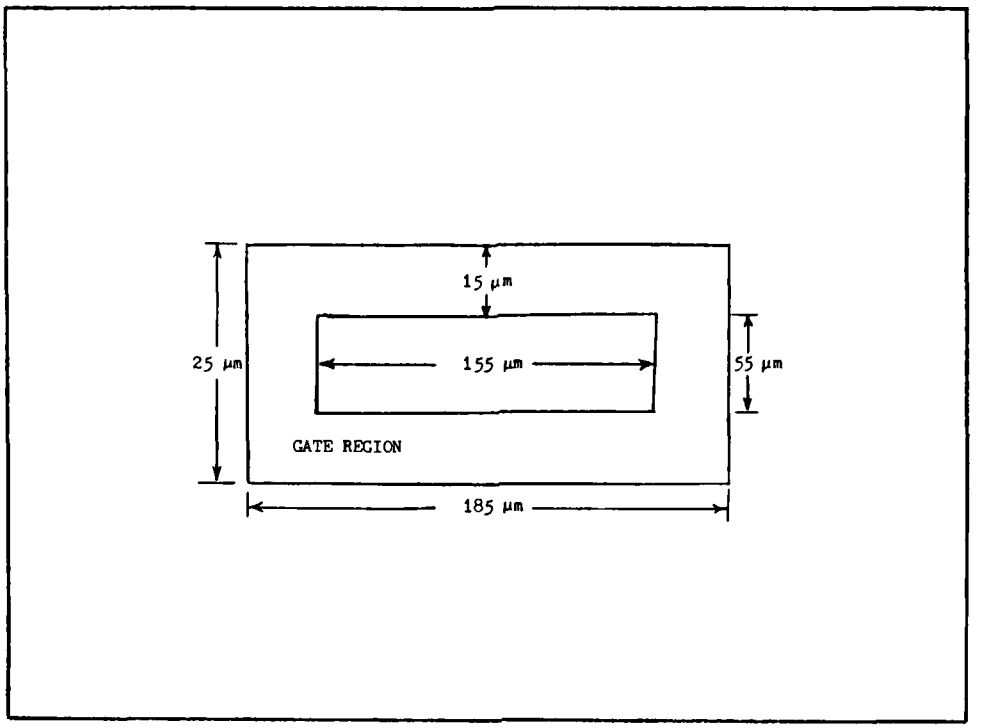


Figure IV-3. Gate Mask Pattern

using cleaning etching solution CL2 (see Appendix B), and the surface resistivity after the gate predep was measured to be 21.2 ohms per square by performing a four-point probe test on the control wafer.

After the four-point probe, the 30 minute gate drive was performed. A bevel and stain was performed on a chip taken from the edge of device wafer A-2. The interferometer photograph shown in Figure IV-4 indicates that the gate had diffused 1.495 microns into the 2.160 microns of epi, thereby establishing a channel width of 0.675 micron at this stage of processing. This is substantially less than the intended one micron channel width required for the desired negative three volt threshold. Never-the-less, processing

continued with the hope that additional diffusion of the gate during subsequent high temperatures would not be severe enough to reduce the pinch-off voltage of the JFET to a value much less than minus one volt.

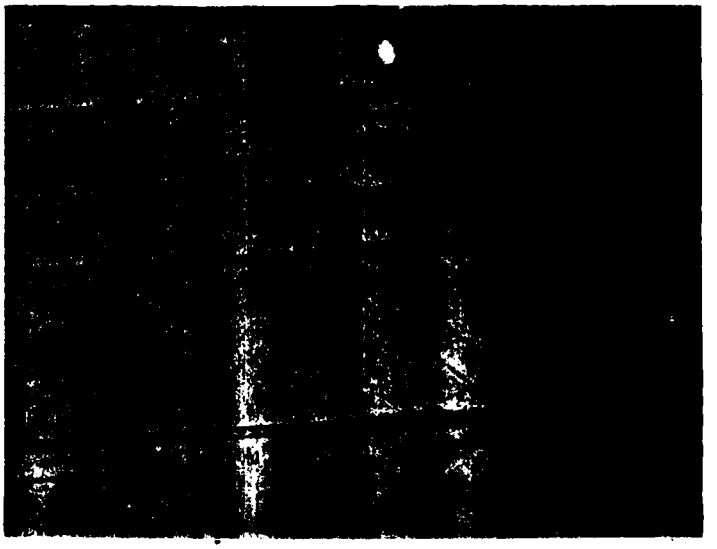


Figure IV-4. Junction Depths of Wafer A-2 after Gate Drive

The oxide grown during the gate drive was determined to be 2450 angstroms thick from an ellipsometer measurement performed on the control wafer after the diffusion. This value is less than the desired goal of 3000 angstroms, however, the text by Colclaser indicates that it should be adequate to mask phosphorous at 1050 degrees C for 30 minutes (Ref 17: 142).

Having completed the gate diffusion, the oxide was again stripped from the surface of the control wafer in

preparation for the next processing step, the source/drain diffusion.

JFET Source/Drain Diffusion. The source/drain diffusion process included the source/drain mask photolithography process, etching of the source/drain pattern, and the enhancement diffusion of the source/drain regions. The actual diffusion was a phosphorous diffusion into the n-type epi to enhance the doping concentration of the source/drain regions to an n+ designation.

The photolithography process was initiated by positioning the source/drain mask (L3) in the mask aligner according the the manufacturer's operating instructions (Ref 31). The source/drain pattern used is shown in Figure IV-5.

The photolithography steps listed in Appendix G were performed to obtain the source/drain pattern which was then etched through the oxide in approximately seven minutes using the procedure outlined in Appendix H.

After etching the oxide pattern, the 15 minute source/drain predep was performed on device wafers A-1 and A-2, followed by a four-point probe of the control wafer AC-1. The post source/drain predep surface resistivity was measured to be 8.54 ohms/square, which should be more than sufficient to achieve ohmic contact with aluminum at the source and drain regions.

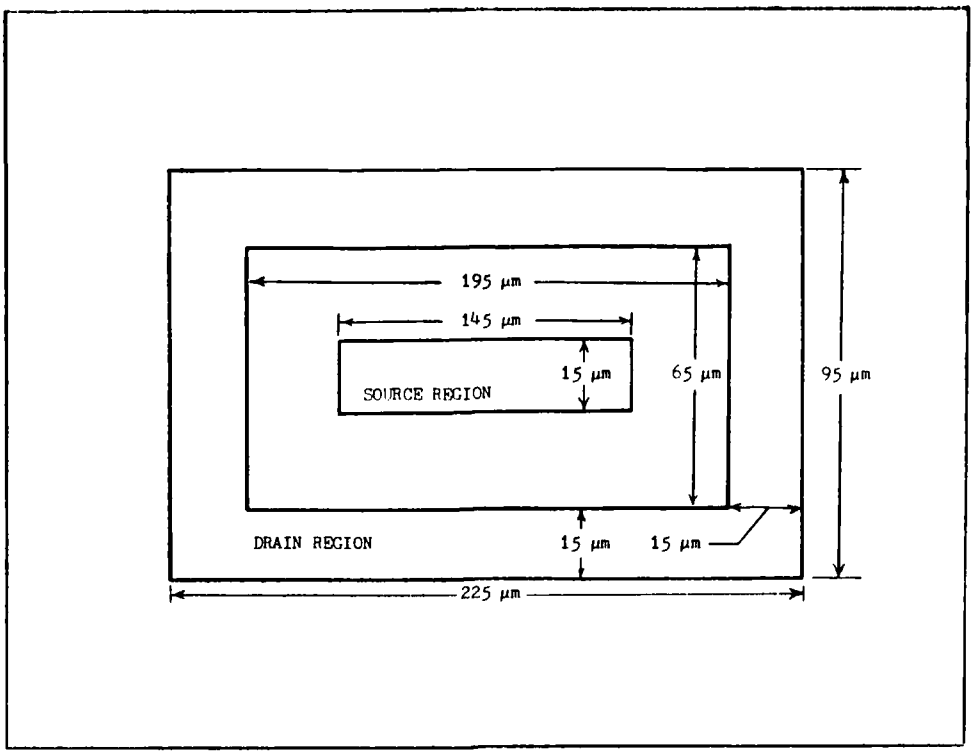


Figure IV-5. Source/Drain Mask Pattern (L3)

With the establishment of an adequate predep, the source/drain was driven for 15 minutes, during which a 4-8-3 minute dry-wet-dry oxidation cycle was used to grow the final oxide through which contact cuts would be etched. Using an ellipsometer, the oxide grown on the control wafer during the source/drain drive was measured to be 1360 angstroms thick. The oxide on the control wafer was then stripped using straight HF, and a subsequent four-point probe revealed the post source/drain surface resistivity to be 5.44 ohms/square, which indicates a surface concentration greater than necessary to achieve good ohmic contact with aluminum.

With the completion of the source/drain diffusion, the

next processing step was to etch the contact windows.

Contact Window Etch. This process involved obtaining the contact window pattern using the contact window mask photolithography process and etching the contact windows through the oxide.

The contact window mask (L4) was positioned in the mask aligner, and the two device wafers were processed using the photolithography procedure outlined in Appendix G, followed by the etching procedures outlined in Appendix H. The wafers were then immediately placed into the oven at 220 degrees C in nitrogen ambient to avoid growing any oxide in the metallization contact cuts. The standard of commercial industry is to limit the elapsed time between contact etch and metallization (in the vacuum chamber) to no more than two hours to prevent evaporating the metal onto too thick of a room temperature grown oxide in the contact cuts (Ref 32).

Limiting surface oxidation of the silicon by minimizing the time between etching the contact windows and placing the wafers in the metallization chamber enhances the chance of ohmic contact between the metal and silicon. In view of these considerations, the 220 degree C dry bake for the subsequent and final photolithography step was reduced from two hours to one hour. With the completion of the contact window process, the wafers were ready for the metallization process.

Metallization Process. The complete metallization process involved the metallization mask photolithography pro-

cess, evaporation of metal onto the wafer surface, lift-off of the metal pattern, and an anneal of the metallized layer.

The photolithography process was initiated by positioning the metallization mask (L5) in the mask aligner. At this point it should be noted that the photolithography process for metallization differs from the previously performed photolithography processes. With the metallization process, no post-bake ("hard-bake") or oxide etch was performed after the PR had been developed.

Since Ballantine encountered much difficulty due to the fact that the PR layer was too thin, Shipley 1350J PR was used instead of the 1470J and the spin speed for PR application was reduced to 4000 RPM. Owing to the fact that a thicker PR layer was involved it was also necessary to increase the exposure time to about 30 seconds and the development time to more than one minute to achieve a satisfactory pattern for metallization. The pattern on one of the two device wafers (A-2) was slightly misaligned, necessitating a reiteration of the photolithography sequence. The PR on wafer A-2 was removed by rinsing it with acetone, but the pattern on wafer A-1 was satisfactory, so it was continued through the metallization process alone.

After developing the metallization pattern, the photolithography process of Appendix G was essentially completed. Wafer A-1 was then placed in the vacuum vapor deposition chamber. The metal deposition equipment consisted of a vacuum deposition chamber manufactured by Consolidated Vacuum

Corp. (Ref 12) and a Sloan metal thickness monitor (Ref 13). The chamber was evacuated to 9×10^{-6} torr and aluminum was evaporated onto the surface of the wafer at a rate of approximately 10 angstroms/sec as indicated by the deposition rate meter (Ref 13). The crystal monitor indicated a frequency change of 1.50 KHz. This value corresponded to a thickness of 1110 angstroms of aluminum as calculated using Equation (IV-1).

$$t = 2 \Delta f \rho^{-1} \qquad \text{(IV-1)}$$

where

t is the thickness of the deposited metal (angstroms),

Δf is the frequency change (Hz), and

ρ is the density of the metal being deposited (g/cm^{-3})

$\rho = 2.7$ for aluminum
$\rho = 10.5$ for silver

Since the biological effects of an aluminum implant in the brain are unknown, it was necessary to cover the aluminum with an evaporated layer of silver. Since aluminum readily oxidizes upon contact with air at room temperature, the silver was deposited without breaking the vacuum by passing a heating current through a separate tungsten boat containing silver. In this case, the frequency change was 5.50 KHz, corresponding to a deposited thickness of 1050 angstroms of silver.

Lift-off of the undesired metal was accomplished by placing a wafer in a petri dish containing acetone. The

metal on the surface of the wafer was agitated by vigorously spraying it with acetone from a squeeze bottle. Since the metal was not satisfactorily lifting off in all places, the dish and wafer were placed in an ultrasonic cleaner for one or two seconds using a low power setting. This caused the metal pattern to tear near the edges and facilitate the acetone reaching the PR to affect lift-off of the metal pattern.

An attempt at probing the wafer for electrical characteristics was made, however the deposited metal was found to be too fragile without first being annealed. Therefore, the wafer was placed in the phosphorous diffusion tube, at a distance very near the opening of the tube which was measured to be at a temperature of approximately 450 degrees C using a thermocouple. After 10 minutes the wafer was removed. Upon inspection with a microscope, the metal pattern was blurred and indistinct. Apparently the metal had reached its melting point (eutectic of 564 degrees C) and destroyed the pattern despite the fact that the surface of the wafer was turned away from the hot zone of the tube (facing the tube opening). Subsequent electrical probing indicated the wafer was now useless.

The second device wafer (A-2) was then taken through its second iteration of photolithography and metallized in a manner identical to that of the previous attempt. The temperature of the center zone of the phosphorous tube was reprofiled to 500 degrees C using its alternate temperature

setting. Wafer A-2 was annealed for 10 minutes and was then electrically probed.

Successful fabrication would be most easily identified by a resistive characteristic on a transistor curve tracer while probing the source and drain connections of a JFET. Upon probing, "opens" were found between the source and drains of each JFET. Increasing the voltage applied between the source and drain resulted in the appearance of a curve trace characteristic of two diodes connected back-to-back which had reached breakdown. This failure indicated the existence of a NPN structure between the source and drain. It was necessary to ascertain the reason for this failure before continuing with the next processing run.

The most probable cause for failure was that the gate region had diffused too deeply into the epi, to the extent that the depletion region of the gate junction with no bias voltage applied had reached the depletion region of the substrate extending into the epi, in effect pinching-off the channel (See Figure III-1). In order to determine if this was indeed the case, a bevel and stain was performed on a chip from the wafer. The gate region had not diffused entirely through the epi layer, but was apparently close enough to the substrate to pinch-off the JFET channel with no bias applied to the gate. In light of this consideration, the next processing run employed shorter diffusion times in all processing steps subsequent to the gate predep to minimize the distance the gate region diffuses into the

epi.

Earlier in this chapter it was mentioned that the surface of the isolation region exhibited the same phenomenon of a spotted appearance similar to that observed by Ballantine (Ref 6: III, 20). What can be termed the "Bubble Anomaly" is shown in Figure IV-6. These bubbles were probably caused by either one or both of the following conditions:

(1) Localized oxidation due to insufficient drying after the prediffusion cleaning process. This is plausible since it is difficult to blow residual water droplets out of the very narrow isolation windows using compressed nitrogen.

(2) Silicon nitride deposits grown during the boron predep of the isolation diffusion.

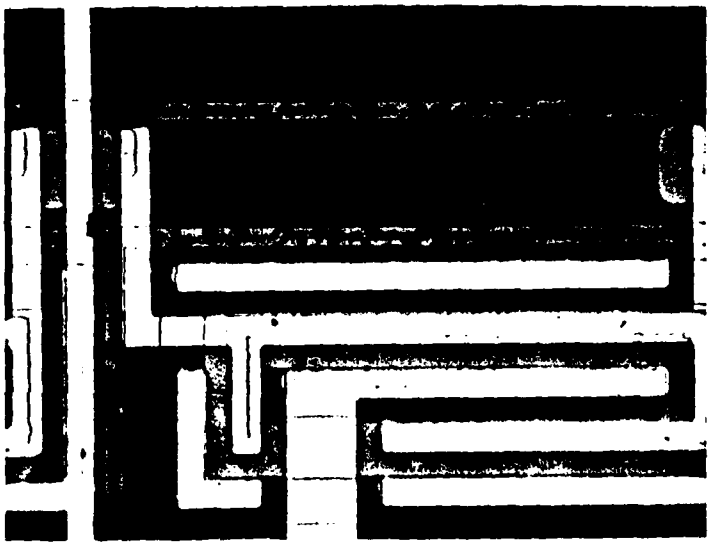


Figure IV-6. Bubble Anomaly of Isolation Diffusion

Through subsequent processing, it was concluded that this anomaly could be eliminated by incorporating the following two steps into the processing runs:

(1) Using a more rigorous nitrogen blow-off after the prediffusion clean.

(2) Using a slight trickle of oxygen (3 to 5%) during the boron predep of the isolation diffusion.

Summary of Second Processing Run

The first processing attempt ended in failure apparently due to the gate region diffusing too deep. In an effort to circumvent this occurrence, the following changes

were instituted in the processing schedule for the second processing run:

(1) 1000 angstroms of dense (dry) plus 2000 angstroms of wet oxide constituted the initial field oxide, grown using an oxidation cycle comprised of 100 minutes dry, 12 minutes wet, and 8 minutes dry growth. This change was made because less oxide thickness prior to the gate diffusion would reduce the amount of silicon epi consumed during oxidation by 0.05 micron, and the increased dry oxide growth period lengthened the time during which the epi diffused into the substrate. The denser oxide also provided a more reliable diffusion mask.

(2) The source/drain drive duration was shortened to 12 minutes, during which a 1900 angstrom oxide was grown using an oxidation cycle comprised of 4 minutes dry, 6 minutes wet, and 2 minutes dry growth. The oxidation time was reduced because more than 1000 angstroms was grown during the final oxidation of the first run. Even with this modification, the thickness grown still surpassed the desired amount.

With the exception of these changes, the actual processing steps executed were very similar to those used for the first run. The details were not included here since this attempt was also unsuccessful. The desired resistive path between the source and drain of each JFET was not present. The previous "open" characteristic was once again encountered.

Events contributing to the failure of this run included the fact that the PR on one wafer lifted off during the isolation oxide pattern etch necessitating re-oxidation of the wafer (2590 angstroms thick) which consumed an additional 0.13 micron of epi. The other wafer suffered from a bad metallization because that the tungsten boat ran out of aluminum while still depositing metal. The metal was stripped using cleaning/etching solution CL5 and the wafer was remetallized. These difficulties add a measure of uncertainty as to the exact cause of failure, but excessive diffusion of the gate junction was still suspected to be the main problem.

Only slight modification of the processing schedule could be justified as a result of this run. The gate predep and drive were already at their minimum. The predep could not be shortened because an adequate surface concentration would not be obtained, and the drive was as short as would permit sufficient time to grow an olide for the required phosphorous diffusion mask. Additionally, the phosphorous predep could not be shortened for fear of not achieving ohmic contact.

Summary of Third Processing Run

The processing schedule used for the third run differed from the previous run in only one respect. The source/drain drive was shortened to only nine minutes, during which 3 minutes of dry, 5 minutes of wet, and 1 minute of dry oxide growth were accomplished. This resulted in an adequate

oxide thickness measured to be 1250 angstroms.

This attempt was also unsuccessful because and "open" existed between the source and drain of each JFET. A bevel and stain performed on each of the device wafers revealed the channel width was about 0.8 micron. This value was close enough to the desired 1.0 micron width to discount failure due channel pinch-off with no gate reverse bias applied.

With no other apparent cause for failure, it was surmised the initial field oxide may not have adequately masked the isolation diffusion. This event would cause a lightly doped p-type region to exist beneath the source and drain regions, producing an effective NPN structure between the two regions. The concentration of the p-type region was apparently so slight that it was not prone to staining.

In light of the considerations developed during this processing run, the isolation diffusion process step was re-examined. In comparison to the 45 minute gate diffusion, 440 minutes for the isolation diffusion seems quite excessive. So the decision was made to shorten the time duration of the isolation diffusion drive used in the next processing run. The exact length of time used for the drive was determined by performing a bevel and stain of a device wafer at intermediate points of the isolation drive during the subsequent processing attempt.

Summary of Fourth Processing Run

In the fourth processing attempt the wafers remained in the oxidation tube for an additional 6 hours (in a nitrogen ambient) after the growth of the initial field oxide, in order to compensate for the subsequently shortened isolation drive. After the isolation predep, a bevel and stain was performed to obtain the photograph shown in Figure IV-7. The fringe lines of the interferometer indicate the boron diffused to a depth of about 0.270 micron. This value is much less than expected, indicating there was apparently a thin layer of oxide remaining in the pattern prior to the predep. The fact that the boron diffused deeper at the outside edges of the isolation windows (see Figure IV-7) supports the hypothesis since the oxide in the windows was determined to be thinner at the edges. This is consistent with the fact that one would expect the DI water used to rinse the HF during the pattern etch to reach the corners or edges of the pattern last. Hence, a greater degree of etching occurs in these areas.

A thickness profile of the surface oxide was obtained using a Sloan Dektak (Ref 33) and confirmed the fact that the window of the isolation region was deepest near the edges, indicating that about 50 angstroms of oxide had been present in the diffusion windows prior to the isolation predep.

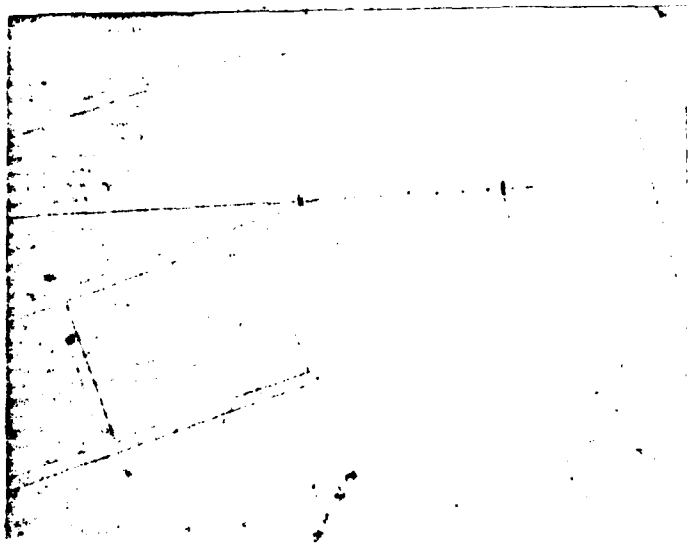


Figure IV-7. Isolation Diffused Depth After Boron Predep

The isolation drive was performed next and was temporarily suspended after 60 minutes in order to perform a bevel and stain to verify the diffused depth of the isolation region. Figure IV-8 shows the diffused depth of the isolation region after the 60 minute drive. The figure indicates the p-type region had not yet diffused completely through the epi. Thus the wafer was placed back in the furnace for an additional 30 minutes of drive time. A bevel and stain was performed on the wafer again and the isolation was found to have diffused completely through the epi as is evidenced by Figure IV-9. No oxide was grown over the isolation region prior to the gate predep since both diffusions used boron, and it was not detrimental if the doping

concentration of the isolation region was enhanced. From this point on, the processing schedule was identical to that which was used for the previous three processing runs.

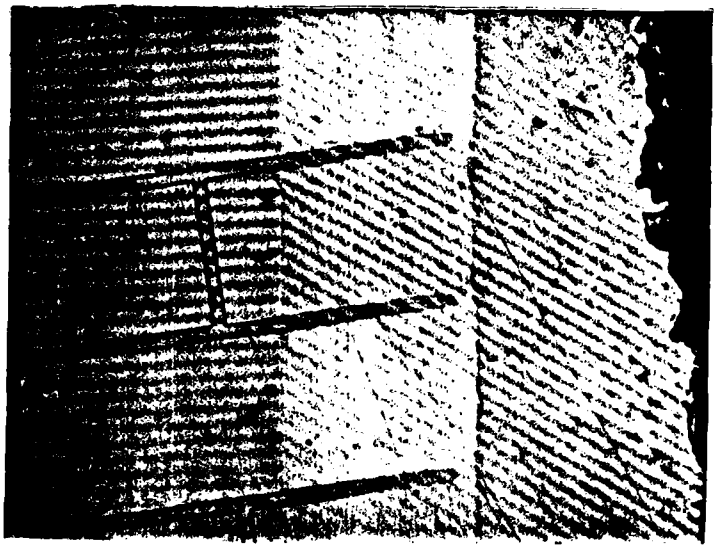


Figure IV-8. Isolation Diffused Depth For 60 Minute Drive.

Probing the device for electrical characteristics yielded test results identical to those of the previous processing runs. A bevel and stain was performed in an attempt to determine the reason for failure. Upon examining the bevelled and stained chip under a microscope, it was

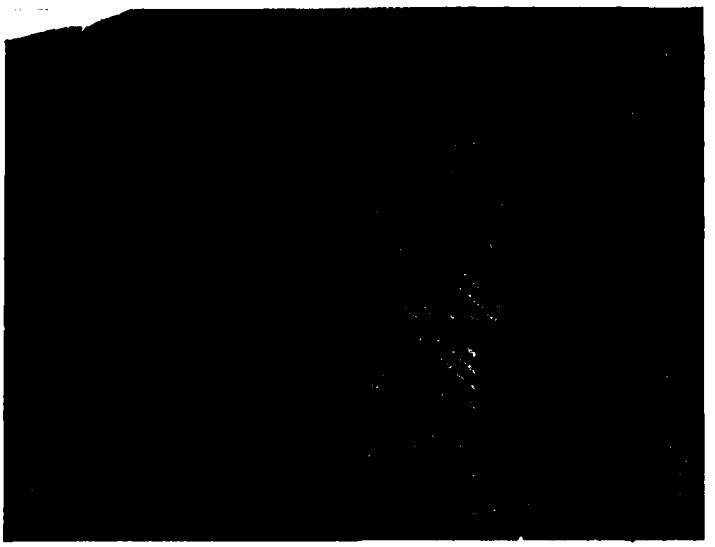


Figure IV-9. Isolation Diffused Depth For 90 Minute Drive

discovered that some of the isolation "wells" in which the JFETS resided were doped p-type (see Figure IV-10). Apparently, some of the photoresist (PR) had lifted off in selected areas prior to etching the gate pattern in the oxide. The PR could have been selectively removed due to a harsh rinse during development. It could also have been blown off while drying the wafer with compressed nitrogen or any other such accident arising from carelessness during processing.

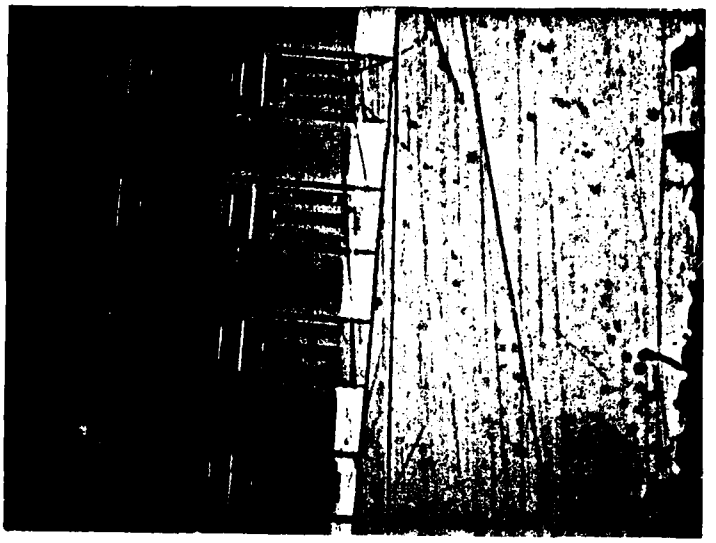
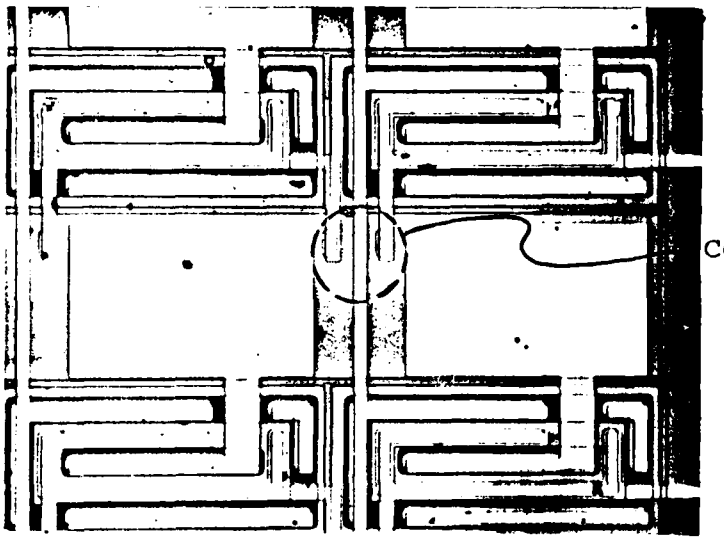


Figure IV-10. Aberration of Gate Diffusion During Run #4.

This unintentional p-type doping of the interior of some of the JFET cells resulted in the formation of an NPN structure between the source and drain of any JFET residing in such a defective isolation well. Since each gate of every JFET in a row is connected in series to its neighbor via a p-type cross-under diffusion (see Figure IV-11), any row containing one such defective device results in all of the gates in that row being connected to the isolation region and substrate. Other than this phenomenon, no other reason for failure of this run can be offered, unless of course bad metallization contact was to blame.



Cross-under Diffusion Connecting Gate Regions of Each JFET in a Row

Figure IV-11. Inter-connection of JFET Gates

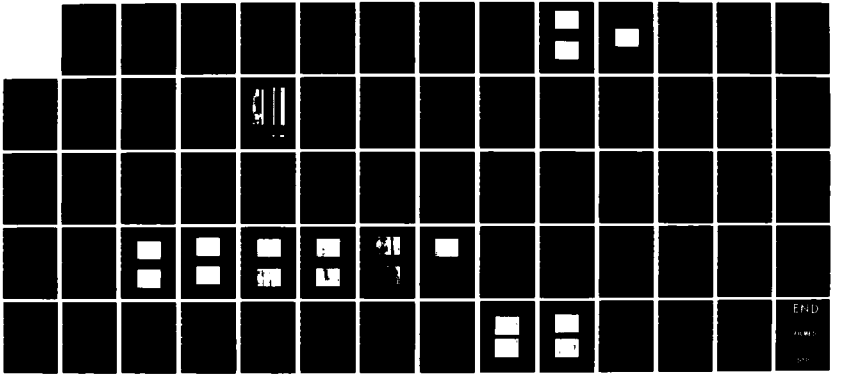
Summary of Fifth and Final Processing Run

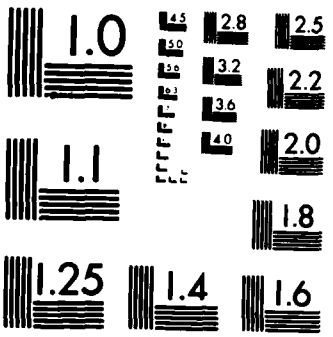
Since the last of the available wafers would be used in this attempt, it was to be the last chance at a successful run. The results of the previous four processing runs were carefully analyzed before any processing commenced on the fifth processing run. After careful deliberation, the following decisions concerning the processing schedule of the final run were made:

(1) The initial field oxide would be comprised of a smaller fraction of dry (dense) oxide and more of the total thickness grown as a result of wet oxidation. This was done because great difficulty was experienced during the previous

AD-A151 803 FABRICATION OF A BIOLOGICALLY-IMPLANTABLE MULTIPLEXED MULTIELECTRODE ARRA..(U) AIR FORCE INST OF TECH WRIGHT-PATTERSON AFB OH SCHOOL OF ENGI.. M E SOPKO 2/2

UNCLASSIFIED DEC 84 AFIT/GE/ENG/84D-63 F/G 9/1 NL





processing runs when attempting to etch the mask pattern through the dense oxide. Long pattern etch times were required, and the PR often did not retain its integrity long enough to etch completely through the oxide. The etchant would undercut the photoresist and cause it to lift off after about five minutes of etch time, which was frequently insufficient to completely etch the pattern. The oxide thickness was also increased from 3000 to 4000 angstroms to preclude the chance of failure due to an insufficient diffusion mask.

(2) A longer nitrogen anneal period was added to the end of the initial field oxide growth cycle to gain additional epi thickness resulting from its diffusion into the substrate. Twelve more hours in a nitrogen ambient at 1050 degrees C was added to the previously used six hours of soak time at the end of the initial oxide growth. Thus, epi drift occurred over an 18 hour time span (not including time spent during field oxide growth) prior to the isolation predep.

(3) No oxide was grown during the isolation drive. This was done to preserve as much epi thickness as possible prior to the gate predep. It also permitted the enhancement of the surface concentration of the isolation region during the gate diffusion.

(4) A thicker oxide was grown during the gate drive. The drive time was increased from 30 minutes to a total of 34 minutes to provide a thicker diffusion mask for the

source/drain diffusion in order to preclude failure due to insufficient masking of the isolation and gate regions (boron diffusions) during the phosphorous diffusion.

Initial Oxidation. With these considerations in mind the final processing run began with the growth of a 4000 angstrom field oxide on three device wafers and one control wafer. The two additional wafers were obtained from separate stock by the same manufacturer. The control wafer utilized was a wafer that had surface bevel and stain cuts performed by the manufacturer. The third device wafer was one that had been rejected by the same manufacturer because slight scratches existed on its surface. The oxidation was performed at 1050 degrees C using a 70 minute cycle comprised of 20 minutes dry O_2, 30 minutes wet O_2 (steam), and 20 minutes dry O_2.

The wafers remained in the oxidation tube in a nitrogen ambient to allow the epi to diffuse further into the substrate to gain as much additional channel width as possible. After six hours, wafer E-3 was removed from the furnace. The other wafers were returned to the furnace for an additional soak of 12 more hours at 1050 degrees C. After removing the remaining wafers from the furnace, the oxide grown on wafer EC-1 was measured to be 3945 angstroms thick using an ellipsometer.

Isolation Diffusion. The isolation mask photolithography steps were performed on the three device wafers (as

listed in Appendix G) followed by the oxide pattern etch (as listed in Appendix H). During the oxide etch the PR on wafer E-3 lifted off, and the pattern was unfortunately destroyed. It was thus necessary to strip the surface of E-3 clear of oxide using straight (undiluted) HF. The wafer was then returned to the oxidation tube and 1210 angstroms of oxide was grown on its surface using 100 minutes of growth time in a dry O_2 ambient at 1050 degrees C. Before removing the wafer from the furnace, it remained in a nitrogen ambient for eight hours to increase the epi junction depth in an attempt to compensate for the silicon consumed during the added oxidation step. The isolation masking was then performed on the wafer again.

The 40 minute isolation predep of boron at 1050° C was performed and the boron glass was stripped using cleaning/etching solution CL2. The 90 minute isolation drive was then performed. Note that no oxide was grown during the drive, and the control wafer was not included in the boron predep.

Gate Diffusion. The gate mask photolithography steps were performed using the procedure listed in Appendix G. The oxide pattern was then etched using the procedure listed in Appendix H. After performing a standard processing clean, the 12 minute gate predep (using boron) was performed at 1050 degrees C. The boron glass was removed using cleaning/etching solution CL2 and a four-point probe of EC-1 revealed the surface resistivity to be 15.9 ohms/square.

The 34 minute gate drive was then performed at 1050 degrees C. During the drive, 4 minutes in dry O_2, 27 minutes in wet O_2, and 3 minutes in dry O_2 were devoted to oxide growth. Using an ellipsometer, the oxide thickness grown on EC-1 during the gate drive was measured to be 2770 angstroms. The oxide on the control wafer (EC-1) was removed using undiluted HF, and the post drive surface resistivity was measured to be 41.6 ohms/square using a four-point probe.

Source/Drain Diffusion. Next, the source/drain mask photolithography steps were performed on the three device wafers. During this phase of processing, wafer E-3 was dropped on the floor and shattered into dozens of small fragments. The remaining two device wafers were then etched. The 15 minute source/drain predep (using phosphorous) was then performed at 1000 degrees C. The predep was immediately followed by the 9 minute drive comprised of 3 minutes of dry O_2, 5 minutes of wet O_2, and 1 minute of dry O_2 devoted to oxide growth. The measured thickness of oxide grown was 1250 angstroms.

Contact Windows. Following the source/drain diffusion, the contact window mask photolithography steps were accomplished, and the oxide pattern was then etched. The metallization mask photolithography process commenced immediately.

Metallization. The metallization mask photolithography process was then performed as with the previous runs. The frequency change during the aluminum deposition was 1.35 KHz which corresponds to a thickness of 1000 angstroms. The

silver deposition evoked a frequency change of 5.80 KHz which corresponds to 1100 angstroms of silver deposited.

Lift-off. The two wafers were each individually placed in a petri dish containing acetone. The metal on the surface of the wafer was agitated by vigorously spraying it with acetone from a squeeze bottle. Since the metal was not satisfactorily lifting off in all places, the dish and wafer were placed in an ultrasonic cleaner for one or two seconds using a low power setting. This caused the metal pattern to tear near the edges and facilitated the acetone reaching the PR to affect lift-off of the metal pattern. Once the pattern was satisfactorily defined, the wafers were annealed at 500 degrees C for 10 minutes.

Evaluation. An initial test was performed using the probe station and transistor curve tracer to measure the V-I characteristics between the source and drain of JFETs from each wafer. Linear, ohmic resistive paths were measured between the sources and drains of JFETs on each wafer indicating success had finally been reached. It was discovered however that the channel of the JFETs on wafer E-1 could not be pinched off regardless of the gate bias applied. Attempts at enhancing channel conduction were also ineffective. These effects are believed to be attributable to either a bad metallization or misalignment during one of the various photolithography phases, since the JFETs of wafer E-2 functioned correctly, and both wafers had evolved through identical processing schedules.

Since success had at long last been realized, it was necessary to electrically characterize the functional devices of wafer E-2 and determine pertinent device parameters. The next chapter describes the testing and evaluation effort.

V. JFET Test and Analysis

Test Procedure Used

In order to measure the electrical parameters of the JFETs, wafer E-2 was placed in the probe station. Four probes were used to contact the JFET's source, gate, drain, and substrate (through the isolation L-bar contact). The probes were then connected to a transistor curve tracer, which was set up to display JFET transistor characteristics. The collector supply polarity was set to that used for an NPN transistor (positive collector supply voltage sweep with emitter grounded). The source, drain, and gate were respectively connected to the emitter, collector, and base jacks of the curve tracer. To maintain consistent measurements, the substrate was connected to ground.

A representative V-I characteristic of a JFET was obtained as shown in Figure V-1, for no applied gate bias (gate grounded to source). The curve indicates that the channel begins to saturate when

$$V_{pO} = V_{DS} = 0.5 \text{ volts}$$

To determine the channel resistance, the linear resistive region of the characteristic curve was examined. The horizontal and vertical scale factors of the curve tracer were changed to magnify this region as shown in Figure V-2. From this figure, the ON-channel resistance (non-saturated) was calculated to be 2.5 kΩ.

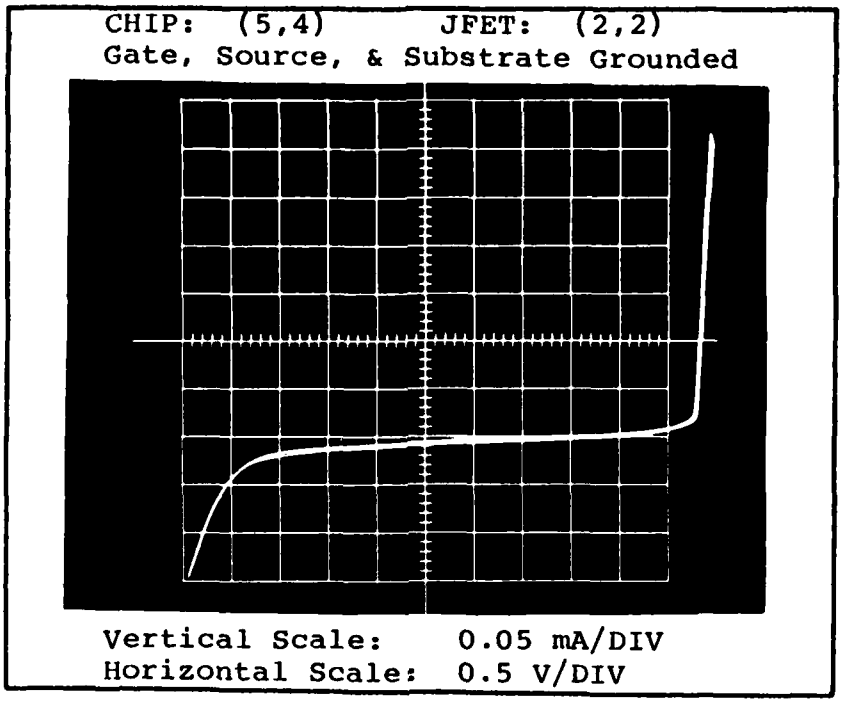


Figure V-1. JFET V-I Characteristic (No Gate Bias)

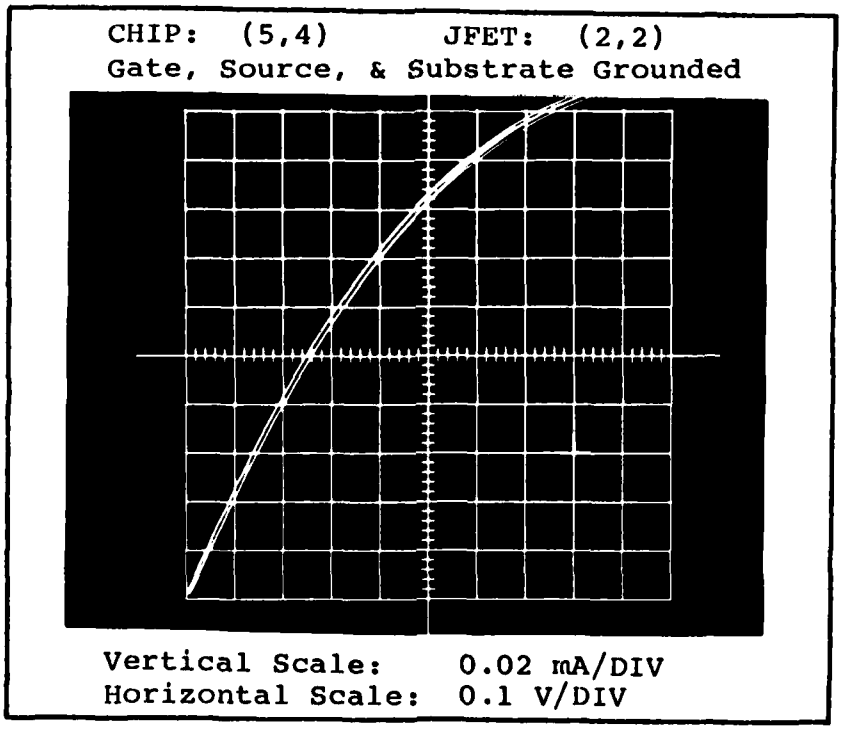


Figure V-2. JFET ON-Channel Resistance

The pinch-OFF voltage was determined by applying an increasingly negative bias voltage to the gate and observing the channel current. Figure V-3 shows the JFET characteristic curves obtained using the step generator of the curve tracer. The JFET is effectively pinched-OFF when a gate bias of

$$V_T = V_{GS} = -1.5 \text{ volts}$$

is applied (threshold voltage).

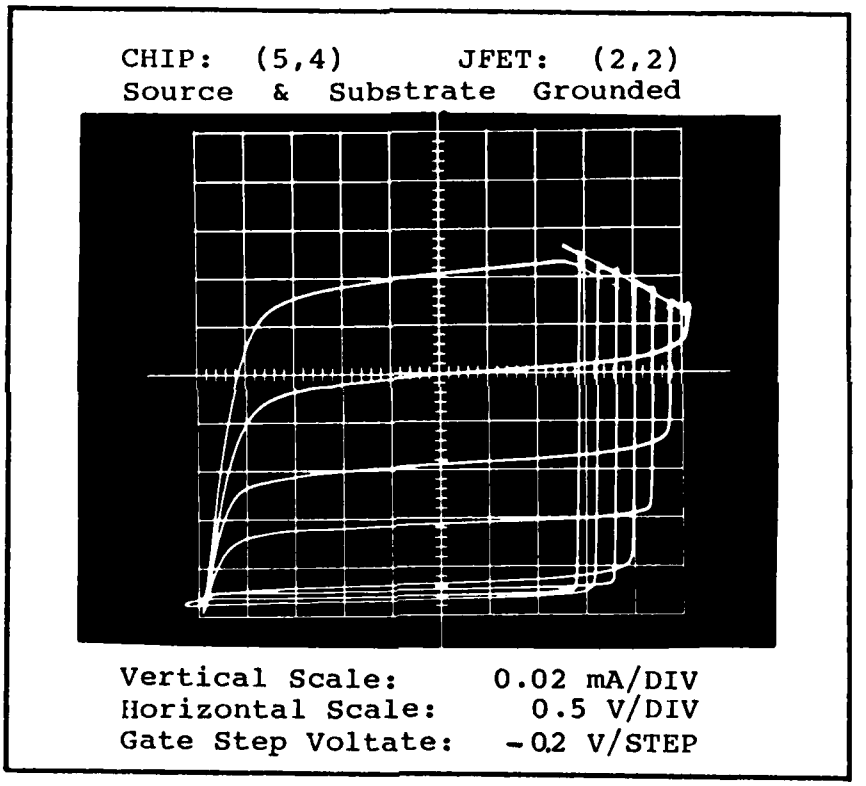


Figure V-3. JFET Characteristic Curves

The Junction leakage current was then measured by reverse biasing selected junctions of the JFET and measuring the current flow through the junction using an ammeter. The leakage test results are listed in Table V-1.

Table V-1. Reverse Bias Junction Leakage Currents

Connection:	GATE	SOURCE	DRAIN	Current (uA)
Junction Voltage Applied :	-3.0 V	0 V	N.C.	5.0
	-3.0 V	N.C.	0 V	5.0
Isolation Leakage Current:				4.9

N.C. = NO CONNECTION

The leakage current across the isolation diffusion was measured by applying 3.0 volts to the source of one JFET and connecting the drain of an adjacent JFET to ground while measuring the current flowing through the circuit. The isolation leakage current was measured to be 4.9 uA. Thus, the reverse leakage current of all junctions was measured to be approximately 5 uA.

Analysis

In order to evaluate device uniformity among the JFETs in a particular chip, as well as from chip to chip, V-I characteristics were obtained for various JFETs at different positions on the wafer. Comparison of the characteristics in Appendix M for various JFET locations shows that there is considerable uniformity among devices from the same chip, but the variation among devices from different chips is considerable, and increases as the separation between chips becomes greater. This is not unusual since the doping concentrations for chips near the center of the wafer are

greater than for those closer to the edges of the wafer.

Results

A summary of electrical parameters for JFETs in the vicinity of the center of the wafer is shown in Table V-2.

Table V-2. Summary of JFET Electrical Parameters.

V_{PO} = 0.5 volts	- Pinch-off Voltage
I_{DSS} = 0.14 mA	- Saturation Current
V_{DSO} = 4.5 volts	- Breakdown Voltage
V_T = -1.5 volts	- Threshold Voltage
I_{RL} = 5.0 uA	- Reverse Leakage Current
R_{ON} = 2.5 kΩ	- ON Channel Resistance

Test Conditions: Source and Substrate Grounded.

VI. Encapsulation and Packaging

Introduction

It was intended that the 16 X 16 JFET array which was fabricated in the lab be passivated or encapsulated with a coating of polyimide to protect the JFET circuitry from the harsh saline environment that it would later be subjected to. It was also planned that the passivated array would be connected to a previously fabricated NMOS multiplexer chip and be mounted in a package suitable for cortical implantation in the skull of a rhesus monkey. Unfortunately, time did not permit the actual encapsulation and packaging of the so called "Brain Chip." In an effort to maintain completeness, however, this chapter presents the packaging scheme which would have been implemented had time permitted.

The proposed packaging scheme for the JFET array relies heavily upon the work done in a concurrent thesis project by Capt. Ricardo Turner (Ref 7). Turner developed a passivation procedure using polyimide for a 16 X 16 NMOS array similar to the JFET array fabricated in this thesis, and a mounting/packaging technique for the NMOS chip. Since the NMOS chip is very similar in nature to the JFET array, the mounting and packaging technique developed by Turner for the NMOS chip, as well as the polyimide passivation procedure, are applicable the JFET array of this thesis.

The packaging scheme for the JFET array involves basi-

cally two processes: (1) Passivation of the JFET array with polyimide, and (2) Mounting the array to the implantable package developed by Turner and interfacing the array to the multiplexer chip. The multiplexer is part of the same chip used in Turner's thesis (Ref 7).

Passivation of the JFET Array

The array passivation procedure involves encapsulating the wafer surface with polyimide and selectively etching the polyimide from the surfaces of the metal sensing electrodes and bonding pads. The encapsulation techniques used by Turner were more applicable to individual chips, but he also developed a procedure for use with three-inch wafers. Since the throughput of encapsulating the arrays on the three-inch wafer is much greater than that of individual chips, it is most advantageous to complete the passivation of the arrays prior to dicing up the wafer into individual chips.

The arrays may be passivated with polyimide as an encapsulant by using the procedure outlined in Appendix K. This is the same procedure as Schedule #3 developed by Turner (Ref 7: A, 5-6). Five such coatings of polyimide should be applied through five successive iterations of the procedure in Appendix N to ensure an adequate passivation layer of polyimide.

After the final cure of the polyimide encapsulant, the wafer is diced into individual chips using a diamond tipped

cylinder using epoxy cement, in an arrangement as shown in Figure VI-3. Once the mounting cement has set, the outputs (S00 - S015) of the multiplexer are connected to the gate bonding pads of the JFET array using an ultrasonic wire bonder. The 16 output columns are connected to the cross section of the wires at the surface of the epoxy filler. The control inputs to the multiplexer, as well as V_{dd} and GND, are also wire bonded to the wires in the epoxy filler of the mount. In addition, the substrate (or L-bar ground plane) is wire bonded to the V_{dd} connection of the multiplexer.

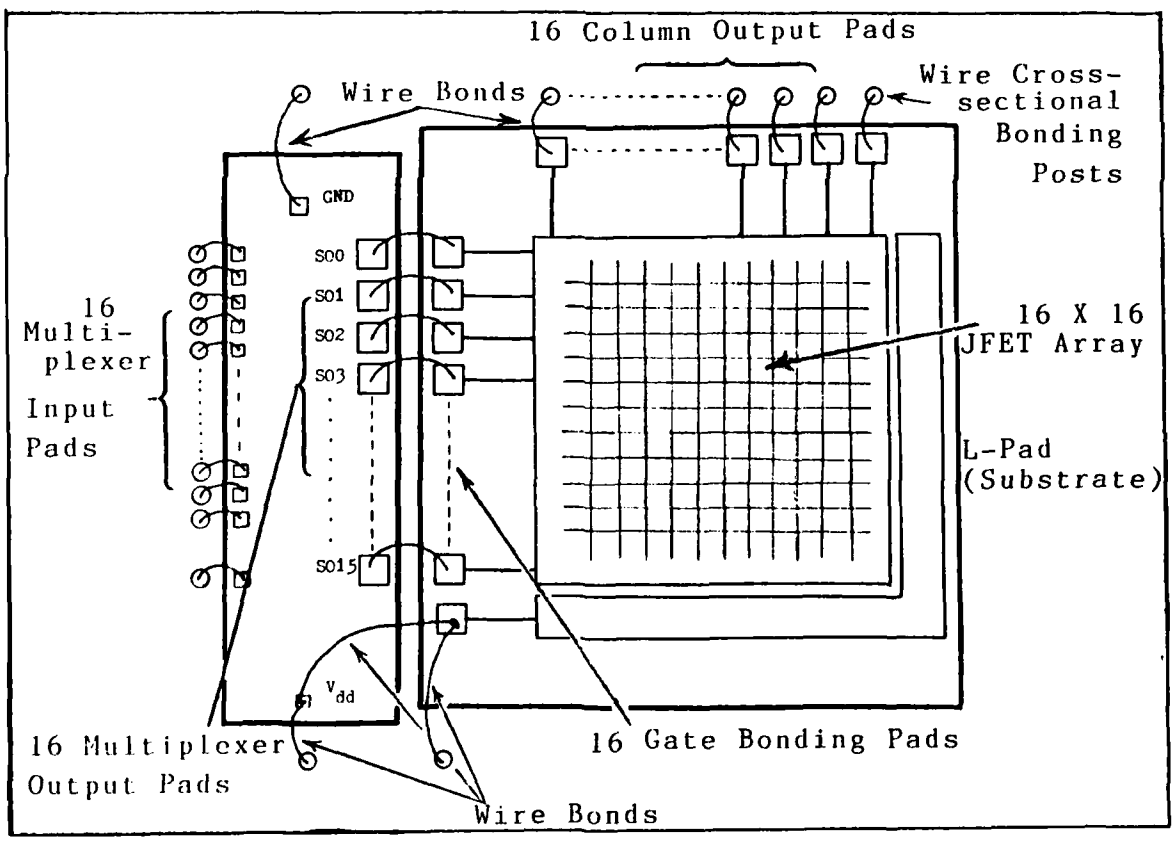


Figure VI-3. Multiplexer/JFET Array Mount

scribe or dicing saw if available. The individual JFET array chips are now ready to be mounted in an implantable package along with the multiplexer chip.

Mounting and Interfacing Array to Multiplexer Chip

Before the passivated JFET array can be connected to the NMOS multiplexer, both the array and multiplexer chip must be mounted in the implantable package developed by Turner. The implantable package (REF 7: II) is basically a hollow metal cylinder filled with epoxy. Wires pass through the epoxy and are connected to a 55-pin connector on one end and terminate at the surface of the epoxy on the other end as shown in Figure VI-1. The details of the fabrication of the mounting package designed by Turner are expounded in the second chapter of his thesis (REF 7: II).

The circuitry of the multiplexer is shown in Figure VI-2. The multiplexer chip itself is obtained by cutting it away from the NMOS array (Multiplexer Design I) of Ballantine's thesis (BA:V-2) using either a diamond tipped scribe or wafer saw. The chip was designed with contact pads at the 16 output connections of the multiplexer to facilitate testing and to permit wire bonding it to another array.

Actual mounting of the Brain Chip is accomplished by butting the multiplexer chip up against the array chip and securing both to the surface of the epoxy filled metal

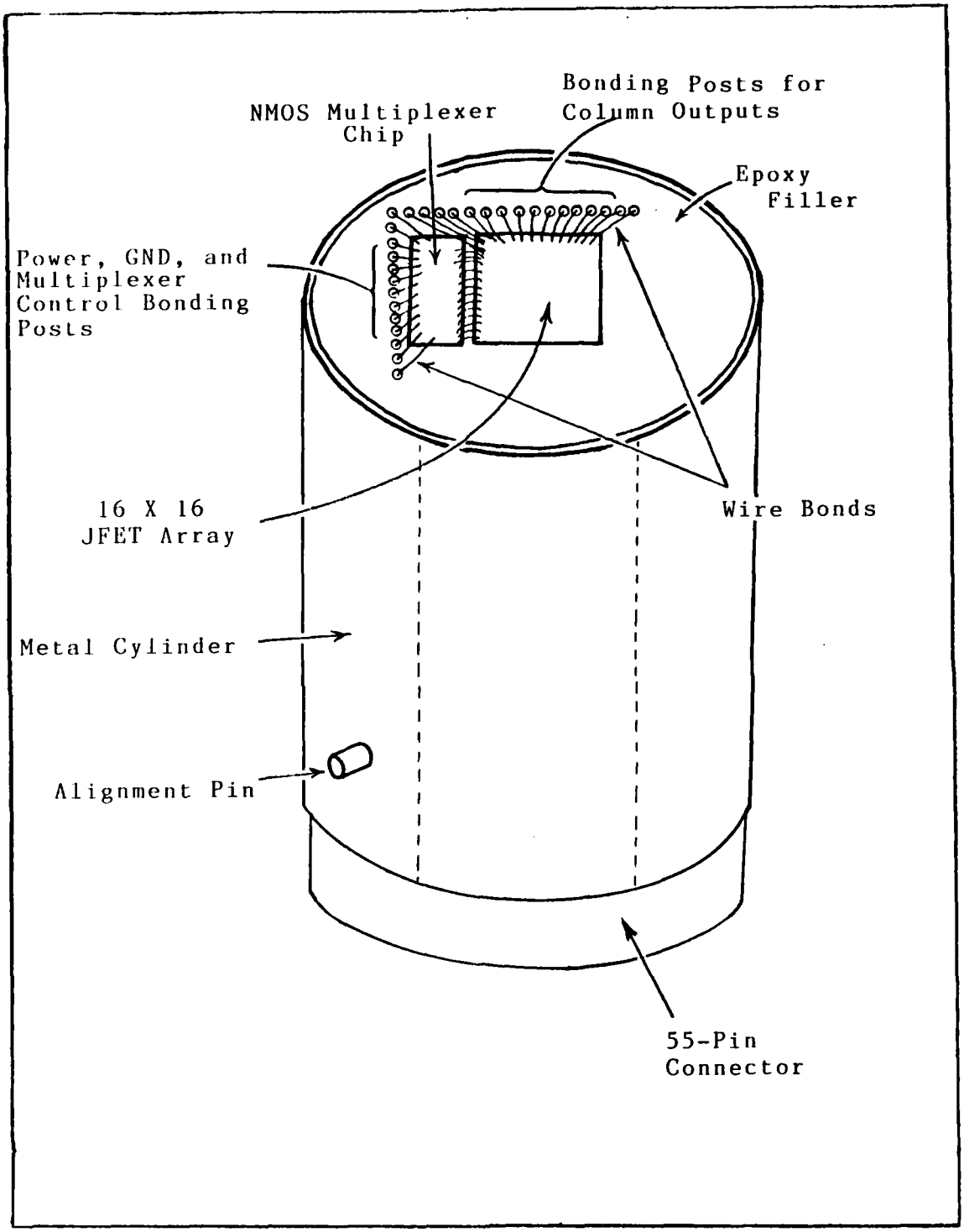


Figure VI-1. Implantable Package

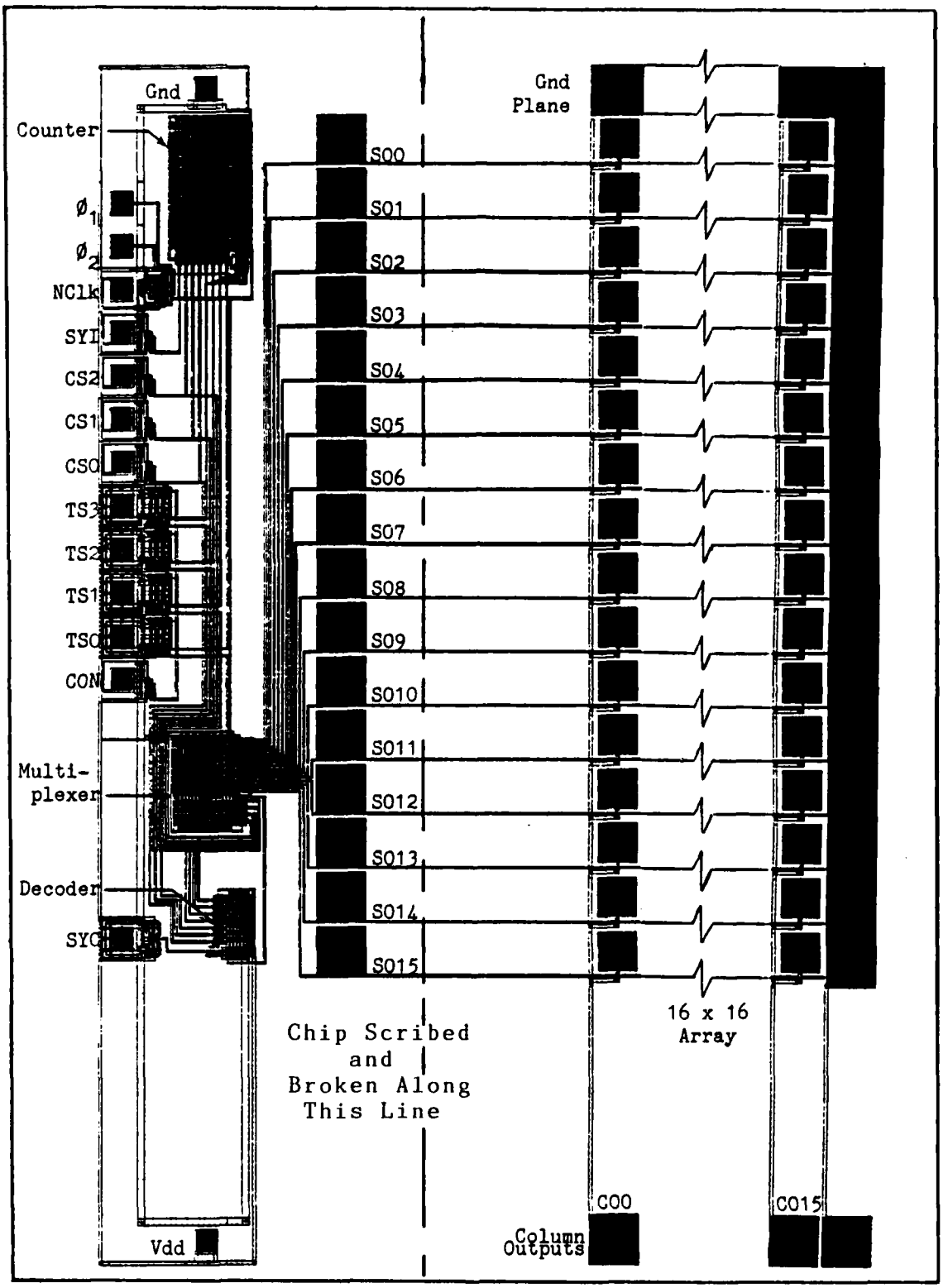


Figure VI-2. Layout of NMOS Multiplexer Design I

After all the bonding pads of both chips have been connected to their respective bonding pads in the mount, epoxy is carefully applied over the entire surface of the mount, exercising care so as not to break any wire bonds. The previously encapsulated JFET array is is NOT covered with epoxy anywhere other than around the edges of the chip and over the wire bonding pads.

Parameters for Operation of Multiplexer and Array

To successfully interface the multiplexer to the array, the multiplexer supply voltage must be applied in a rather unconventional way. The V_{dd} connection of the NMOS multiplexer (which is also connected to the L-bar ground plane and substrate of the JFET array) must be grounded during operation, and the multiplexer connection labeled GND must be connected to -4 volts as shown in Figure VI-4. This negative supply voltage is necessary in order to always cause one output of the multiplexer to be zero while all the others go to approximately -4 volts, thus pinching-off the JFETs in all rows to which a negative gate bias is applied. This allows the voltage sensed at the JFET sources of only the selected row (zero or positive voltage applied to the gate) to be read at the 16 column output pads.

The supply voltage must not exceed -4 volts to ensure an adequate margin of operation below the JFET avalanche breakdown voltage (approximately 4.5 volts), and it must be

greater than -3 volts in order to ensure adequate pinch-off disabling the the JFETs in an unselected row.

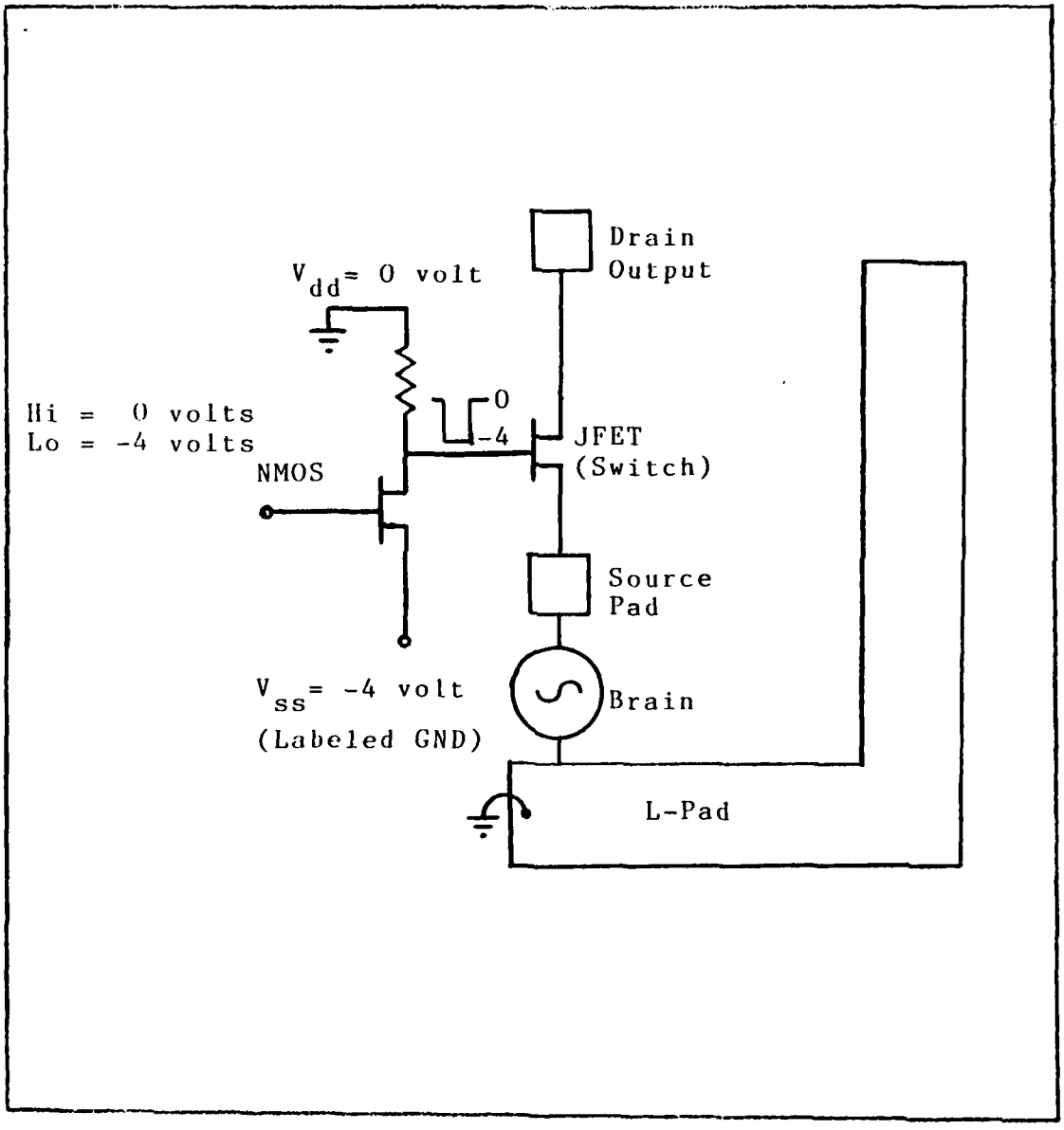


Figure VI-4. Multiplexer/JFET Array Interface

VII. Conclusions and Recommendations

Conclusions

The transistor characteristic curves obtained during tests of the Brain Chip array attest to the fact that it is indeed possible to fabricate Junction Field Effect Transistors under the somewhat "less than ideal" conditions of the AFIT Cooperative Electronic Materials and Processes Laboratory. A processing schedule capable of producing functional JFETs in an environment below Class 100 clean room standards has been developed and proven to be successful.

Cleanliness Standard. It was possible to achieve successful photolithography patterns despite the fact that fabrication took place under conditions below Class 100 clean room standards. The use of positive rather than negative photoresist is credited as being the main reason for the realization of successful patterns in conjunction with the fact that the device geometries involved (five micron minimum line width) were not especially critical. Dust was observed on both the wafer surface as well as on the photolithography mask, but the relatively thick photoresist layers and long ultraviolet exposure times resulted in patterns with almost no visible defects under a microscope using dark-field illumination.

Diffusion contaminants did apparently pose a problem since the reverse leakage current of the device junctions

was rather high, despite the fact that HCl gettering and backside gettering techniques were employed. The high leakage may be attributable to the fact that as time elapsed over the course of the five processing runs, the processing environment may have become more contaminated subsequent to the initial clean which was performed prior to the the first processing attempt. As time progressed, tedium may also have induced some degree of carelessness during processing.

Processing Schedule. The lack of exact agreement between the diffused junction depths measured during processing and those predicted by pre-fabrication calculations can largely be attributed to the difficulty in determining accurate values of the diffusion coefficients used in the calculations. Additionally, the complimentary error function and Gaussian equations used to approximate the concentration profiles of the diffusions are not an exact representation of the actual diffusion mechanism in a practical sense.

Even so, the error connected with the estimated diffused junction depths was not so gross as to prevent an adequate baseline for an initial processing schedule. Also, the short time durations of the high temperature diffusions introduced great uncertainty as to the actual amount of time spent at the desired temperature since the wafer insertion and withdrawal times were significant in comparison to the diffusion times.

The use of a two micron epitaxial layer was extremely restrictive in the development of an adequate processing

schedule. The major objective of schedule development was minimizing the total gate diffusion time. The limiting factors to post gate predep processing were the time required to grow a sufficiently thick oxide to provide an adequate diffusion mask for the phosphorous diffusion and the need for a substantial phosphorous predep to achieve an acceptable surface concentration prior to contact metallization.

Evaluation of Array Produced. The JFET array which was finally fabricated possessed parameters satisfactory for use with the NMOS multiplexer. The devices were also characterized as having a good deal of uniformity on individual chips and an acceptable amount of uniformity from chip to chip. However, the limited tests performed on the array in this thesis cannot be considered conclusive enough to establish that the array fabricated is adequate for actual cortical implantation and data collection.

The test set-up employed in this thesis was geared toward establishing uniformity of the devices produced and a standard evaluation procedure which would afford consistency among measurements. The devices were not intended to be operated with the JFET sources tied to the grounded substrate. It is therefore necessary to evaluate the operation of the chip with the substrate grounded and the JFET sources connected to a signal on the order of 50 to 1000 microvolts (typical of the signals encountered at the surface of a

mammalian brain) before concluding that the chip is worthy of the effort required to package and interface it to the multiplexer. Additionally, further in vitro testing, similar to that performed by Turner, is needed before surgically implanting the Brain Chip.

Recommendations

Prior to formulating any conclusive judgements concerning the practicality of the array fabricated in this thesis for actual biological data collection, further testing should be conducted to evaluate the operation of the chip/multiplexer interface and the ability of the chip to sense voltage levels on the order of 100 to 1000 microvolts.

The use of wafers with a thicker epitaxial layer would greatly improve the flexibility of a new processing schedule. Wafers with a four micron epitaxial layer should aid in the development of a processing schedule which is much more forgiving and fault tolerant than that which was employed in this thesis.

The use of low temperature predepositions should result in greater predictability and repeatability concerning diffused junction depths. The time length of the predep can be increased to achieve doping concentrations comparable to those of this thesis with a less significant amount of diffusion occuring during the predep. The wafer insertion and withdrawal times also become less significant in comparison to the longer predep.

In the event that wafers with a thicker epitaxial layer and the desired epi and substrate concentrations are not available, the following suggestions are offered when using wafers like the ones in this thesis effort:

(1) Use sputtering, which is a low temperature process, to deposit post gate diffusion oxides

(2) Lowering the gate predep temperature and increasing the duration of it to achieve the desired surface concentration.

To further reduce leakage due to sodium contamination, the use of a chlorine-bearing compound as a gettering agent during dry oxide growth in addition to use during wet growth is advised. Also, extreme care should be exercised when handling wafers at all times, and the amount of dead time between processing steps should be maintained at an absolute minimum. Alternatively, processing may be accomplished at a fabrication facility which has Class 100 or better cleanliness.

The amount of aluminum deposited during metallization should be reduced to about 500 angstroms, and the thickness of the silver layer should be increased to 2000 angstroms. This action requires the spin speed for application of the pre-metallization photoresist be reduced to thicken the photoresist layer. The anneal temperature should also be increased to about 525 degrees C for 10 minutes to sufficiently toughen the contact pads for probing because 500 degrees C was found to be inadequate.

The most beneficial advice that could be offered to

anyone desiring to pursue a fabrication attempt similar to this one is that dry run attempts of all processing phases, especially metallization, be performed using scrap or dummy three-inch wafers prior to the actual attempt involving a good device wafer.

Bibliography

1. Kabrisky, Mathew. A Proposed Model for Visual Processing in the Human Brain. Urbana: University of Illinois Press, 1966.

2. Tatman, Joseph A. A Two-Dimensional Multielectrode Microprobe for the Visual System. MS Thesis. Wright Patterson AFB, Ohio: School of Engineering, Air Force Institute of Technology, December 1979. (AD A080378).

3. Fitzgerald, Gary H. The Development of a Two-Dimensional Multielectrode Array for Visual Perception Research in the Mammalian Brain. MS Thesis. Wright-Patterson AFB, Ohio: School of Engineering, Air Force Institute of Technology, December 1980. (AD A100763).

4. German, George W. A Cortically Implantable Multielectrode Array for Investigating the Mammalian Visual Cortex. MS Thesis. Wright-Patterson AFB, Ohio: School of Engineering, Air Force Institute of Technology, December 1981.

5. Hensley, Russel W., and David C. Denton. The First Cortical Implant of a Semiconductor Multielectrode Array; Electrode Development and Data Collection. MS Thesis. Wright-Patterson AFB, Ohio: School of Engineering, Air Force Institute of Technology, December 1982.

6. Ballantine, Robert B. The Development and Fabrication of an Implantable, Multiplexed, Semiconductor Multielectrode Array. MS Thesis. Wright-Patterson AFB, Ohio: School of Engineering, Air Force Institute of Technology, December 1984.

7. Turner, Ricardo R. Encapsulation and Packaging of a Semiconductor Multielectrode Array for Cortical Implantation. MS Thesis. Wright-Patterson AFB, Ohio: School of Engineering, Air Force Institute of Technology, December 1984.

8. Grove, A. S. Physics and Technology of Semiconductor Devices. New York: John Wiley and Sons, 1967.

9. Zaininger, K. H., and F. R. Heiman. "The C-V Technique nas an Analytical Tool, Part I," Solid State Technology, 13: 49-56 (May 1970).

10. Zaininger, K. H., and F. R. Heiman. "The C-V Technique nas an Analytical Tool, Part II," Solid State Technology, 13: 46-55 (June 1970).

11. Hofstein, S. R. "Stabilization of MOS Devices," Solid State Electronics, 10: 657-670 (July 1967).

12. ----- "High Vacuum Chamber Type CV-18 Instruction Manual." Consolidated Vacuum Corporation.

13. _____ "Deposit Thickness Monitor DTM-2a Installation and Operation Manual." Sloan Instruments.

14. ----- "C-V Plotter Model 410." Princeton Applied Research.

15. Monkowski, J. "Role of Chlorine in Silicon Oxidation, Part I," Solid State Technology, 22: 58-61 (July 1979).

16. Monkowski, J. "Role of Chlorine in Silicon Oxidation, Part II," Solid State Technology, 22: 113-118 (August 1979).

17. Colclaser, Roy A. Microelectronics: Processing and Device Design. New York: John Wiley and Sons, 1980.

18. Kriegler, R. J. "The Uses of HCL and Cl2 For the Preparation of Electrically Stable SiO2," Semiconductor Silicon: 363-375.

19. Shiraki, Hiromitsu. "Suppression of Stacking Fault Generation in Silicon Wafer by HCl Added to Dry O2 Oxidation," Japanese Journal of Applied Physics, 15: 83-86 (January 1976).

20. Shiraki, Hiromitsu. "Stacking Fault Generation Suppression and Grown-In Defect Elimination in Dislocation Free Silicon Wafers by HCl Oxidation," Japanese Journal of Applied Physics, 15: 1-10 (January 1976).

21. Dolny, Gary F., Professor of Electrical Engineering. Personal interview. Wilkes College, Wilkes-Barre, Pennsylvania, 1983.

22. ----- "Production Ellipsometer 1117 for Measurement of Surface Film Thickness and Refractive Index." Bulletin EA-77, Gaertner Scientitfic Corporation.

23. ----- "Ellipsometric Tables for Thin Films of Silicon at Wavelength 6328A." Gaertner Sicentific Corporation, 1975.

24. ----- "Digital Resistivity Test System Model 1900, Instruction Mod-1900." The Micromanipulator Co.

25. ----- "PDS Boron Nitride High Temperature Planar Diffusion Sources (BN-1100 and BN-1250) Technical Data." The Carborundum Company, Graphite Products Division.

26. Doyle, Edward and Bill Morris (Editors). Microelectronics Failure Analysis Techniques. A Procedural Guide, sponsored by the Air Force Systems Command, RADC, Griffiss Air Force Base. Syracuse: Electronics Laboratory, General Electric Co., 1983.

27. Sze, S. M. VLSI Technology. New York: McGraw Hill Book Company, 1983.

28. ----- "Phosphorous N-Type Planar Diffusion Source Grade PH-1000 Technical Data." The Carboruncum Company, Graphite Products Division.

29. Glaser, Arthur B., and Gerald E. Subak-Sharpe. Integrated Circuit Engineering. Menlo Park: Addison-Wesley Publishing Company, 1979.

30. Phillips, Alvin B. Transistor Engineering. Malabar: Robert E. Krieger Publishing Company, 1981.

31. ----- "Model CA-2020 Wafer to Mask Alignment and Exposure System Operating and Maintenance Manual." Computervision Cobilt Division.

32. Salley, Edward J. Processing Engineer. Private correspondence. Unitrode Corporation, Lexington, Massachusetts, 1984.

33. _____ "Dektak Surface Profile Measuring System Operating and Maintenance Instructions." Sloan Instruments, June 1980. (M-611(d)-680).

34. ----- "AZ Photoresist Process Instructions." Shipley Company Inc.

APPENDIX A

PREPARING THE DIFFUSION FURNACE

The oxidations and diffusions of this thesis were performed in a Type 410C Diffusion Furnace manufactured by Thermco Products Co. for three-inch wafers. Each of the three furnace tubes (oxidation, p-type, and n-type) were profiled to establish a flat temperature zone at the following temperatures: 1050°C for the initial oxide tube, 1050°C for the p-type (boron) tube, and 1000°C for the n-type (phosphorous) tube.

Each tube has three separate heating zones: the Center Zone and two End Zones. The two End Zones are individually refered to as the Load Zone (farthest from gas source) and Source Zone (nearest to gas source). The three separate temperature zones of each tube are each respectively controlled by separate Ana-lock controllers.

An external thermocouple was placed inside the tube to accurately measure the temperature during adjustment of the three zones. When placed inside the tube, the thermocouple was only long enought to extend five and one-half inches past center. Hence, an 11 inch flat zone (5 1/2 inches left and right of center) was used. The thermocouple was positioned in the tube so the end of the thermocouple as at the center of the tube. The controllers were set to their lowest settings, and power was applied to the tube. The center zone temperature was then slowly increased until the

thermocouple indicated the desired temperature of the tube. Five minutes were allowed after making the adjustment to allow the temperature to stabilize before noting the thermocouple reading. The controls for the center zone were continually adjusted until the temperature reading remained stable within 0.2 degrees of the specified tube temperature.

After the desired Center Zone temperature was attained, the thermocouple was inserted five and one-half inches further into the tube. The controller for the Source Zone was then continually adjusted until it was within 0.2 degrees of the Center Zone temperature. After each adjustment, five minutes were allowed for temperature stabilization as before. The thermocouple was then withdrawn 11 inches and the temperature of the Load Zone was adjusted using the same procedure followed for the Source Zone. The temperature along the 11 inch flat zone was then measured and verified to be within 0.2 degrees of the specified temperature.

It should be noted that the oxide quartz tube was broken at the source end requiring that it be replaced with a new tube before profiling that tube of the furnace. The new tube which was installed was first degreased and cleaned in the following manner prior to installation in the furnace:

(1) Rinsed thoroughly with trichloroethylene

(2) Rinsed thoroughly with acetone

(3) Rinsed thoroughly with methanol

(4) Rinsed thoroughly with deionized (DI) water

(5) Rinsed thoroughly with SC1 (see Appendix K)

(6) Rinsed thoroughly with DI water

(7) Rinsed thoroughly with 10:1 diluted hydrofluoric acid (10 parts DI water : 1 part HF).

(8) Rinsed thoroughly with DI water

(9) Rinsed thoroughly with SC2 (see Appendix K)

(10) Rinsed thoroughly with DI water

After profiling each of the tubes to the specified temperatures, the furnace was ready for processing.

APPENDIX B

CLEANING/ETCHING SOLUTIONS AND USES

The following is a list of the cleaning and etching processes used during this fabrication. Ratios for mixing chemical solutions are provided rather than specific amounts since container size determines the actual amount needed.

CL1: This cleaning process uses sulfuric acid (H_2SO_4), hydrogen peroxide (H_2O_2), deionized water (DIW), hydrofluoric acid (HF), and nitrogen (N_2).

3:2, H_2SO_4:H_2O_2	15 minutes
DIW rinse	15 minutes above 10 megohms
10:1, DIW:HF	15 seconds
DIW rinse	5 minutes above 10 megohms
N_2 blow dry	as required

The first solution is self-heating, which generates a bubbling action when mixed, and is used primarily on new wafers to remove any organic materials that may be present. The second solution is used to remove any inorganic materials, primarily silicon dioxide, from the new wafers.

CL2: This cleaning process uses nitric acid (HNO_3), DIW, HF, and N_2.

HNO_3 (boiling @ 120°C)	30 minutes
DIW rinse	5 minutes above 10 megohms
10:1, DIW:HF	10 seconds

DIW rinse	5 minutes above 10 megohms
N_2 blow dry	as required

The boiling nitric is used to remove the borosilicate glass layer formed on the wafer surface during the boron predeposition. The second solution removes any oxide from the wafer surface that may have grown during the nitric bath.

CL3: This cleaning process uses DIW, HF, and N_2.

10:1 DIW:HF	10 seconds
DIW rinse	5 minutes above 10 megohms
N_2 blow dry	as required

This solution is used to clean the wafer surface of any contaminants and oxide that may have accumulated on the wafer surface during, or between, processes.

CL4: This cleaning process uses ammonium fluoride (NH_4F), HF, DIW, and N_2.

6:1, NH_4F:HF	as required
DIW rinse	5 minutes above 10 megohms
N_2	as required

This solution is used to remove the oxide in the mask pattern. After mixing the solution, it should stand for two hours to stabilize prior to use (very important). Normally it etches silicon dioxide at a rate of approximately 1000 angstroms per minute. The solution is a buffered slolution,

and is therfore more gentle on the photoresist than CL3.

CL5: This cleaning process uses DIW, phosphoric acid (H_3PO_4), HNO_3, and glacial acetic (HAc).

19:17:1:1, DIW:H_3PO_4:HNO_3:HAc	as required
DIW rinse	5 minutes above 10 megohms

This solution is used to remove all the metal from the wafer in the event the metallization process must be reaccomplished. To use, place the solution on a hot plate and heat to 60-65 degreees C.

APPENDIX C

Ballantine's Processing Schedule

This appendix summarizes the frabrication processing steps used in Ballantine's thesis (Ref 6 :F-1).

1. Silicon Wafers: Microwave Associates Inc., (MA/COM).
   a. Substrate: p-type, (100), 20 mils, 40 Ohm-cm.
   b. Epitaxial Layer: n-type, 2 microns, 0.9 ohm-cm.
2. Source Wafers: PDS, Graphite Products Division Carborundum Co.
   a. Boron Nitride, grade BN-1100, 3" x 0.050".
   b. Phosphorous, grade PH-1000, 3" x 0.060".
3. Furnace Preparation: Thermco Products Co., three-inch.
   a. Oxidation Tube: 1050° C; N_2, dry O_2, and wet O_2 at one atmosphere pressure, one liter per minute flow rate.
   b. P-type Tube: 1050° C; N_2, dry O_2, and wet O_2 at one atmosphere pressure, one liter per minute flow rate.
   c. N-type Tube: 1000° C; N_2, dry O_2, and wet O_2 at one atmosphere pressure, one liter per minute flow rate.
4. Initial Oxide: 5000 angstroms.
   a. Initial Wafer Cleaning: Cleaning/etching solution CL1.
   b. Oxidation tube.
   c. Cycle Times: 20 minutes dry O_2, 48.6 minutes wet O_2, 20 minutes dry O_2.
   d. Push/pull: First two feet in/last two feet out at one foot per minute.
   e. Bevel and Stain: Check epi diffusion.
   f. Measure Oxide with Ellipsometer: First and last

wafers in boat.

5. Isolation Diffusion: Boron Source.

   a. Surface Cleaning: Cleaning /etching solution CL3.

   b. Isolation mask photolithography process.

   c. Etch Isolation Pattern: Cleaning/etching solution CL4.

   d. P-type Tube: Predeposition.

   e. Cycle Time: 40 minutes Dry N_2.

   f. Push/pull: First two feet in/last two feet out at one foot per minute.

   g. Remove Borosilicate Glass: Cleaning/etching solution CL2.

   h. Remove Oxide in Pattern: Cleaning etching solution CL3.

   i. Four-point Probe: Check predep resistivity.

   j. Bevel and Stain: Check epi and isolation diffusion depths.

   k. Surface Cleaning: Cleaning/etching solution CL3.

   l. P-type Tube: Drive

   m. Cycle Time: 6 hours, 40 minutes dry N_2.

   n. Push/pull: First two feet in/last two feet out at one foot per minute.

   o. Four-point Probe: Check drive resistivity.

   p. Bevel and Stain: Check epi and isolation diffusion depths.

6. Gate Diffusion: Boron Source.

   a. Surface Cleaning: Cleaning /etching solution CL3.

   b. Gate mask photolithography process.

   c. Etch Gate Pattern: Cleaning/etching solution CL4.

   d. P-type Tube: Predeposition.

e. Cycle Time: 15 minutes Dry N_2.

f. Push/pull: First two feet in/last two feet out at one foot per minute.

g. Remove Borosilicate Glass: Cleaning/etching solution CL2.

h. Remove Oxide in Pattern: Cleaning etching solution CL3.

i. Four-point Probe: Check predep resistivity.

j. Bevel and Stain: Check epi and gate diffusion depths.

k. Surface Cleaning: Cleaning/etching solution CL3.

l. P-type Tube: Drive and gate oxide.

m. Cycle Time: 1 hour, 40 minutes dry N_2, 4 minutes dry O_2, 23 minutes wet O_2, 3 minutes dry O_2.

n. Push/pull: First two feet in/last two feet out at one foot per minute.

o. Four-point Probe: Check drive resistivity.

p. Bevel and Stain: Check epi and gate diffusion depths.

q. Check field oxide.

7. Source/drain Diffusion: Phosphorous Source.

a. Surface Cleaning: Cleaning /etching solution CL3.

b. Source/drain mask photolithography process.

c. Etch Source/Drain Pattern: Cleaning/etching solution CL4.

d. N-type Tube: Predeposition.

e. Cycle Time: 15 minutes Dry N_2.

f. Push/pull: First two feet in/last two feet out at one foot per minute.

g. Four-point Probe: Check predep resistivity.

h. Bevel and Stain: Check epi, gate, and source/drain diffusion depths.

i. Surface Cleaning: Cleaning/etching solution CL3.

j. N-type Tube: Drive and source/drain oxide.

k. Cycle Time: 4 minutes dry O_2, 12 minutes wet O_2, 4 minutes dry O_2.

l. Push/pull: First two feet in/last two feet out at one foot per minute.

m. Bevel and Stain: Check final epi, isolation, gate, and source/drain diffusion depths.

8. Contact Window Openings:

a. Surface Cleaning: Cleaning/etching solution CL3.

b. Contact window mask photolithography process.

c. Etch Contact Window Pattern: Cleaning/etching solution CL4.

9. Metallization: Consolidated Vacuum Corp. vacuum chamber.

a. 500 angstroms aluminum.

b. 500 angstroms silver.

c. Metal lift off.

APPENDIX D

JUNCTION STAINS AND TECHNIQUES

The following is a listing of the junction stains used in this thesis and the techniques employed in their use.

3-1 Stain. The chemical composition of this stain is:

3 parts by volume nitric acid (HNO_3)

1 part by volume hydrofluoric acid (HF)

10 parts by volume acetic acid (HAc)

Within 4 to 5 seconds after a drop of the solution has been applied to the sample, the junctions will appear (p-type regions darken). Lightly doped regions can be brought out by using a light to speed up the reaction. Normally, this stain will, if used for an extended period of time, define all the junctions in a silicon wafer. The use of this stain is recommended only as a last resort, since it also acts as a silicon etchant.

10-1 HF Stain. The chemical composition of this stain is:

1 part by volume HF

10 parts by volume deionized water (DIW)

A drop of the solution is applied to the sample, which is then exposed to a strong microscope light for at least 5 minutes. Lightly doped regions may require much more time to stain. P-type regions darken.

Straight HF Stain. The chemical composition of this stain is:

Undiluted HF (HF assay 49%)

The technique employed with this solution is the same as that for the 10-1 stain, except that only one to two minutes are required to stain the junctions.

APPENDIX E

BEVEL AND STAIN PROCEDURE

A small piece of sample wafer or a circuit die is first obtained by breaking a small (about 4 mm square) piece from a wafer edge using a diamond tipped scribe. The sample is mounted on the beveled side of a lapping cylinder (preferably a one degree bevel) using black wax. To mount the sample, the cylinder is heated on a hot plate and black wax is touched to its surface until the wax melts. When the wax is molten, the sample is placed on the was, and positioned with the wooden end of a Q-tip such that the part of the sample to be beveled is mounted flush to the center edge on the lapping cylinder. The specimen and cylinder are flooded with deionized water (DIW) until cool to solidify the wax. The excess wax is removed with acetone and wiped with a disposable Kimwipe.

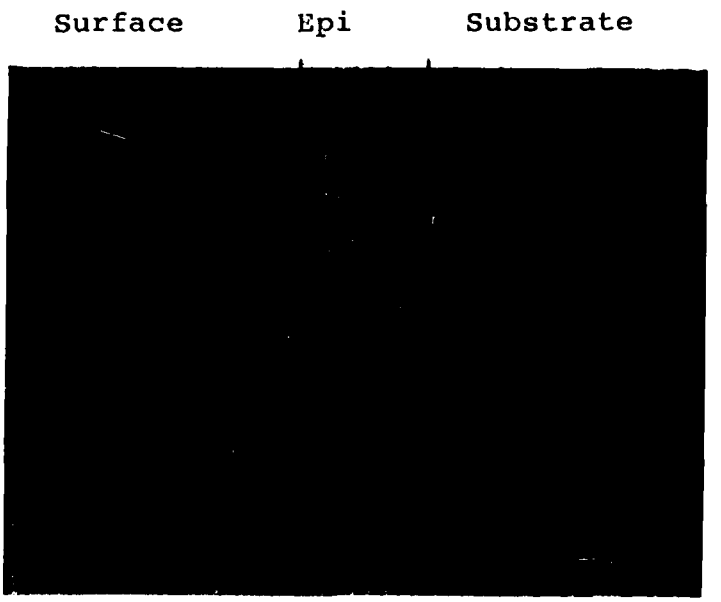
With the sample mounted, the cylinder is screwed on the lapping weight and the assembly is carefully placed into the lapping weight holder. The whole assembly is placed into the lapping tank after squirting some lapping oil (mixture of SHELL PELLA 911 and 0.3 micron alumina powder) on the glass plate. Using parallel strokes, the sample is ground back and forth in the tank for about 50 strokes. The cylinder and lapping weight are then removed from the tank and holder.

The surface of the sample is then scrubbed with acetone using a Kimwipe. One of the stains listed in Appendix D is then applied to the sample while observing it under a microscope. After dark regions appear on the beveled area, the sample is flooded with DIW to quench the HF staining.

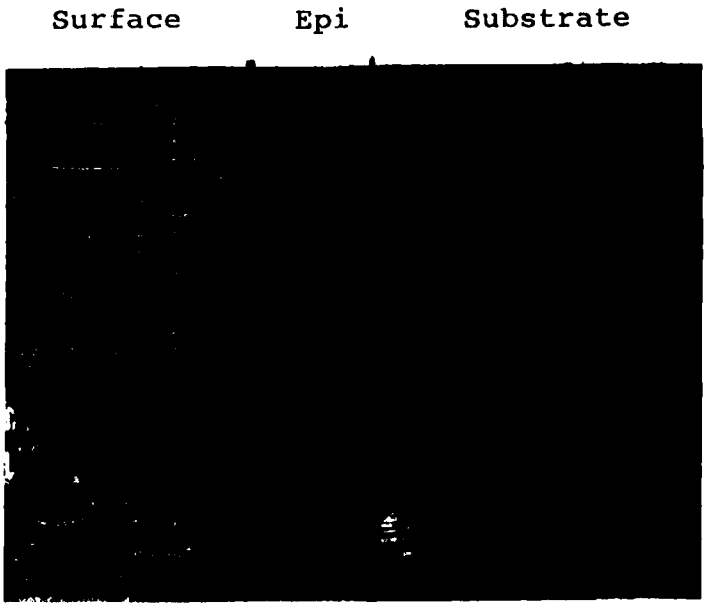
The diffused junction depths can now be determined by observing the sample under a microscope which has an interferometer and camera attached to it. The interferometer causes fringe lines (due to constructive and destructive wave interference of the light source) to appear that can be rotated until they are perpendicular to the edge of the bevel. As the lines cross the bevel, they drop off at an angle. Noting that each fringe line is equal to 2700 angstroms, the width of a particular area can be measured by counting the number of fringe lines crossing the area of interest.

APPENDIX F

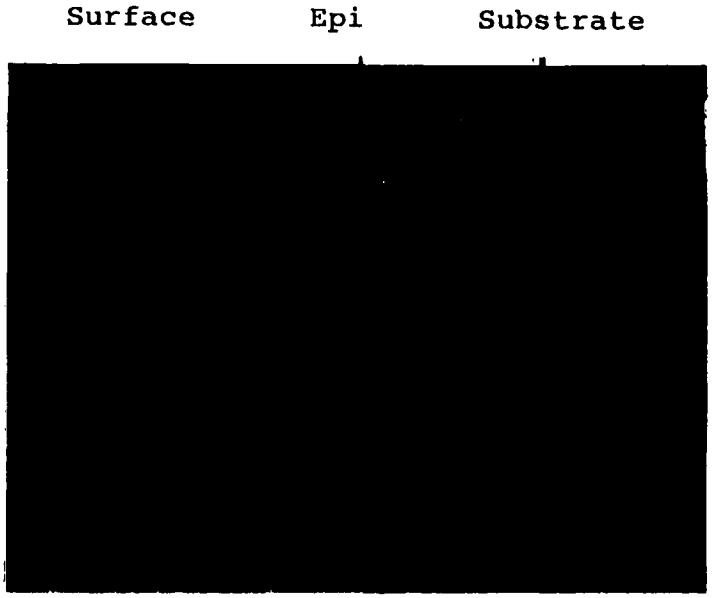
JUNCTION PHOTOGRAPHS FOR DIFFUSION TRIALS



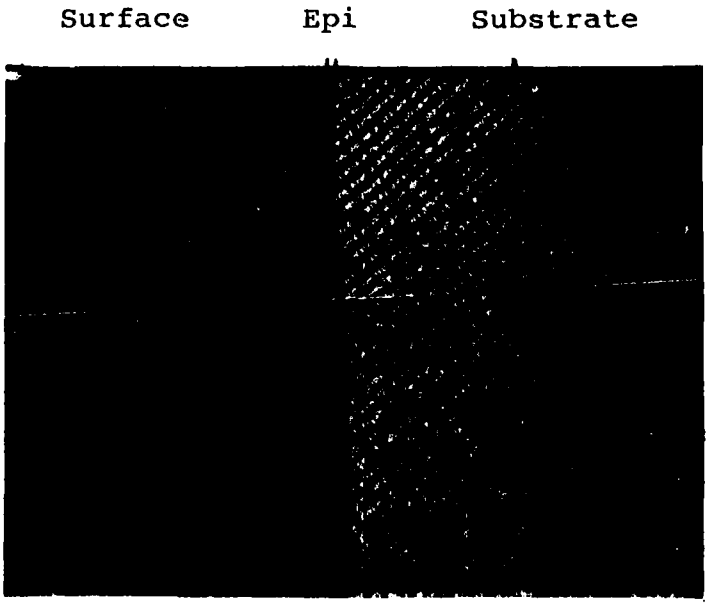
Initial Epi After 4000 A Oxide Grown



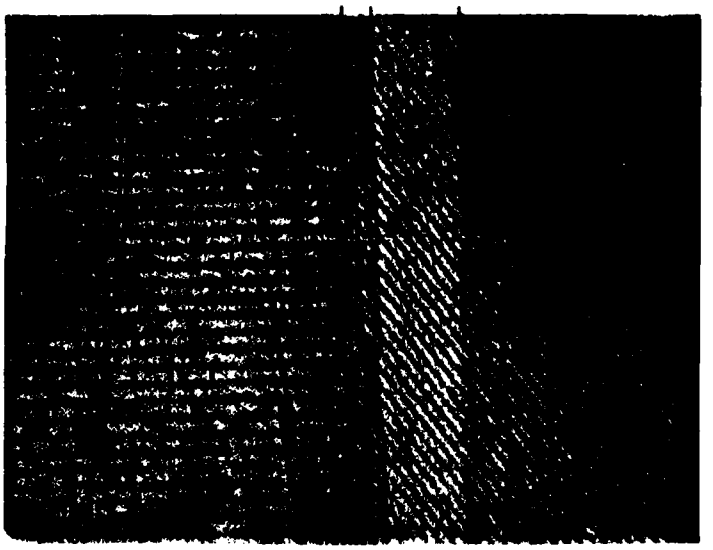
Initial 4000 A Oxide Removed



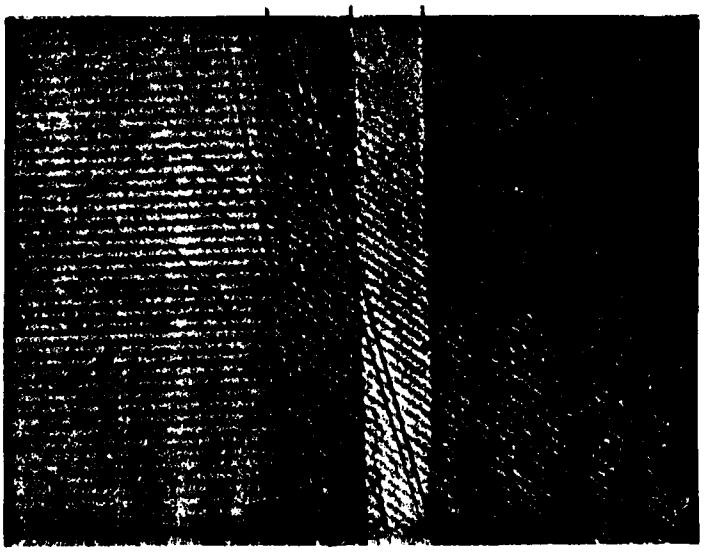
Epi After 440 min. Isolation Drive
(No Impurity Doping and No Additional Oxide Grown)



Junction Depth After 12 Min. Boron Predep

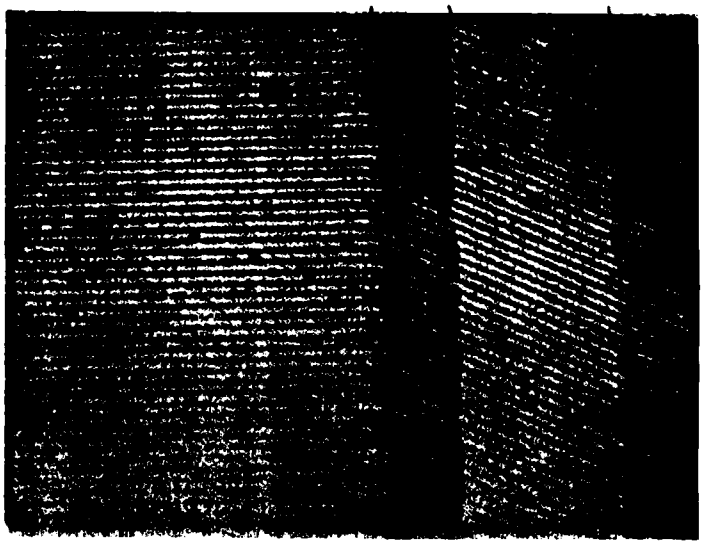


Junction Depth After 12 Min. Boron
Predep + 30 Min. Drive



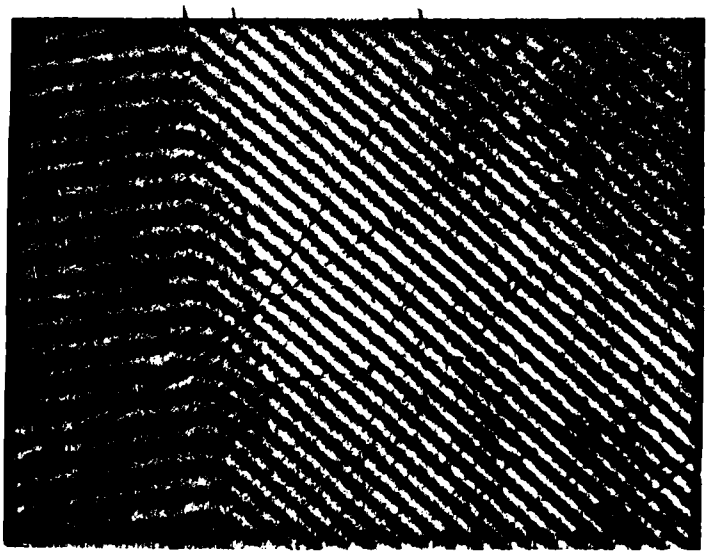
Junction Depth After 12 Min. Boron
Predep + 40 Min. Drive

Surface Epi Substrate



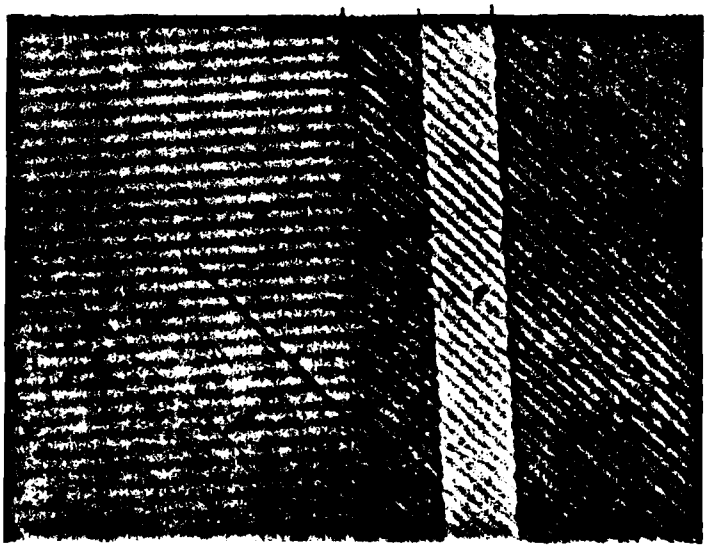
Junction Depth After 12 Min. Boron
Predep + 30 Min. Drive + 15 Min. Phosphorous Predep

Surface Epi Substrate



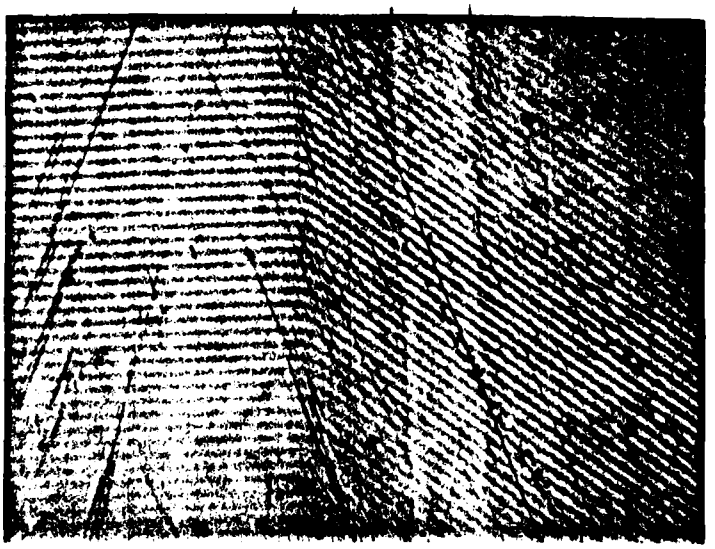
Junction Depth After 15 Min. Boron Predep

Surface Epi Substrate



Junction Depth After 15 Min. Boron
Predep + 30 Min. Drive

Surface Epi Substrate



Junction Depth After 15 Min. Boron
Predep + 40 Min. Drive

Surface Epi Substrate

Junction Depth After 15 Min. Boron
Predep + 30 Min. Drive + 15 Min. Phosphorous Predep

APPENDIX G

STANDARD POSITIVE PHOTORESIST PHOTOLITHOGRAPHY PROCESS

The photoresist used was Microposit™ Photoresist 1470 (1350J for metallization), Shipley Co., Inc. The following procedure is based upon their recommendations (Ref 34).

1. Preheat two ovens: left oven- 220° C;
   right oven- 70° C.

2. Dry wafer-- 220° C for minimum of 1 hour, N_2 ambient.

3. Remove from oven and allow to cool (approximately 5 minutes).

4. Blow clean with N_2.

5. Apply Hexamethyldisilasane adhesion promoter (HMDS):
   - puddle 4 -5 drops on wafer
   - spin/spread @ 6000 rpm for 15 seconds

6. Apply positive photoresist (AZ1350J for metallization or AZ1470 for all other mask levels):
   - puddle 8 - 10 drops on wafer
   - spin/spread @ 6000 rpm for 15 seconds

7. Prebake photoresist-- 70° C for 20 minutes.

8. Blow clean with N_2.

9. Align/expose-- 20 seconds under ultraviolet light.

10. Develop photoresist:
    - puddle AZ351 developer (mixed 1:4 with DIW) onto wafer
    - develop for 60 seconds
    - rinse with DIW
    - GENTLY blow dry with nitrogen
    - examine pattern under microscope and repeat development steps as necessary until no photoresist remains in windows of pattern

11. Post-bake photoresist-- 150 degrees C for 30 minutes to dry and toughen photoresist.

12. Etch oxide pattern (see Appendix H).

NOTE: For the metallization photolithography, reduce the spin speed to 4800 RPM to apply a thicker layer of photoresist.

APPENDIX H

OXIDE ETCHING PROCEDURE

1. Mix sufficient quantity of cleaning/etching solution CL4 to cover wafer, depending upon container size.

2. Allow solution to stand for 2 hours.

3. Place the wafer in the solution and etch for the time required to etch completely through the oxide thickness noting that the etch rate is approximately 1000 angstroms per minute.

4. Remove the wafer from the etch, rinse throughly in running DIW (about 10 seconds), gently blow dry with nitrogen, and examine the pattern under a microscope.

5. If the pattern is not completely clear of oxide, repeat etchings at 15 second increments until all pattern oxide is removed.

6. After completion of the pattern etch, remove all of the photoresist with acetone (scrubbing with a cotton swab if necessary), rinse the wafer with methyl alcohol, and then rinse with running DIW for about 10 seconds.

APPENDIX I

INITIAL PROCESSING SCHEDULE

This appendix summarizes the frabrication processing steps used for the first processing run.

1. Silicon Wafers: Microwave Associates Inc., (MA/COM).
   a. Substrate: p-type, (100), 20 mils, 40 Ohm-cm.
   b. Epitaxial Layer: n-type, 2 microns, 0.9 ohm-cm.
2. Source Wafers: PDS, Graphite Products Division Carborundum Co.
   a. Boron Nitride, grade BN-1100, 3" x 0.050".
   b. Phosphorous, grade PH-1000, 3" x 0.060".
3. Furnace Preparation: Thermco Products Co., three-inch.
   a. Oxidation Tube: 1050° C; N_2, dry O_2, and wet O_2 at one atmosphere pressure, one liter per minute flow rate.
   b. P-type Tube: 1050° C; N_2, dry O_2, and wet O_2 at one atmosphere pressure, one liter per minute flow rate.
   c. N-type Tube: 1000° C; N_2, dry O_2, and wet O_2 at one atmosphere pressure, one liter per minute flow rate.
4. Initial Oxide: 4000 angstroms.
   a. Initial Wafer Cleaning: Standard Processing Clean.
   b. Oxidation tube.
   c. Cycle Times: 40 minutes dry O_2, 30 minutes wet O_2, 20 minutes dry O_2.
   d. Push/pull: First two feet in/last two feet out at one foot per minute.
   e. Measure Oxide with Ellipsometer: First and last wafers in boat.
   f. Remove control wafer oxide using undiluted HF.

5. Isolation Diffusion: Boron Source.

   a. Surface Cleaning: Standard Processing Clean.

   b. Isolation mask photolithography process.

   c. Etch Isolation Pattern: Cleaning/etch solution CL4.

   d. P-type Tube: Predeposition.

   e. Cycle Time: 40 minutes Dry N_2.

   f. Push/pull: First two feet in/last two feet out at one foot per minute.

   g. Remove Borosilicate Glass: Cleaning/etching solution CL2.

   h. Four-point Probe: Check predep resistivity on control wafer.

   i. Bevel and Stain: Check epi and isolation diffusion depths on chip from edge of device wafer.

   j. Surface Cleaning: Standard Processing Clean.

   k. P-type Tube: Drive

   l. Cycle Time: 6 hours and 20 minutes dry N_2, 3 minutes dry O_2, 13 min. wet O_2, and 4 min. dry O_2.

   m. Push/pull: First two feet in/last two feet out at one foot per minute.

   n. Bevel and Stain: Check epi and isolation diffusion depths on chip from edge of device wafer.

   o. Check oxide thickness grown on control wafer.

   p. Remove oxide grown on control wafer using undiluted HF.

6. Gate Diffusion: Boron Source.

   a. Surface Cleaning: Standard Processing Clean.

   b. Gate mask photolithography process.

   c. Etch Gate Pattern: Cleaning/etching solution CL4.

   d. P-type Tube: Predeposition.

   e. Cycle Time: 12 minutes Dry N_2.

f. Push/pull: First two feet in/last two feet out at one foot per minute.

g. Remove Borosilicate Glass: Cleaning/etching solution CL2.

h. Four-point Probe: Check predep resistivity on control wafer.

i. Bevel and Stain: Check epi and gate diffusion depths using control wafer.

j. Surface Cleaning: Standard Processing Clean.

k. P-type Tube: Drive and gate oxide.

l. Cycle Time: 3 minutes dry O_2, 25 minutes wet O_2, and 2 minutes dry O_2.

m. Push/pull: First two feet in/last two feet out at one foot per minute.

n. Four-point Probe: Check drive resistivity on control wafer.

o. Bevel and Stain: Check epi and gate diffusion depths on control wafer.

p. Check field oxide thickness grown on control wafer.

q. Remove oxide grown on control wafer using undiluted HF.

7. Source/drain Diffusion: Phosphorous Source.

a. Surface Cleaning: Standard Processing Clean.

b. Source/drain mask photolithography process.

c. Etch Source/Drain Pattern: Cleaning/etching solution CL4.

d. N-type Tube: Predeposition.

e. Cycle Time: 15 minutes Dry N_2.

f. Push/pull: First two feet in/last two feet out at one foot per minute.

g. Four-point Probe: Check predep resistivity on control wafer.

h. Bevel and Stain: Check epi, gate, and source/drain diffusion depths on control wafer.

i. Surface Cleaning: Standard Processing Clean.

j. N-type Tube: Drive and source/drain oxide.

k. Cycle Time: 4 minutes dry O_2, 8 minutes wet O_2, 3 minutes dry O_2.

l. Push/pull: First two feet in/last two feet out at one foot per minute.

m. Bevel and Stain: Check final epi, isolation, gate, and source/drain diffusion depths.

8. Contact Window Openings:

a. Surface Cleaning: Cleaning/etching solution CL3.

b. Contact window mask photolithography process.

c. Etch Contact Window Pattern: Cleaning/etching solution CL4.

9. Metallization: Consolidated Vacuum Corp. vacuum chamber.

a. Surface Cleaning: Cleaning/etching solution CL3.

b. Metallization mask photolithography process.

c. 500 angstroms aluminum.

d. 500 angstroms silver.

e. Metal lift off.

APPENDIX J

FINAL REVISED PROCESSING SCHEDULE

This appendix summarizes the frabrication processing steps of the final revised processing schedule used for the fifth processing run.

1. Silicon Wafers: Microwave Associates Inc., (MA/COM).
   a. Substrate: p-type, (100), 20 mils, 40 Ohm-cm.
   b. Epitaxial Layer: n-type, 2 microns, 0.9 ohm-cm.
2. Source Wafers: PDS, Graphite Products Division Carborundum Co.
   a. Boron Nitride, grade BN-1100, 3" x 0.050".
   b. Phosphorous, grade PH-1000, 3" x 0.060".
3. Furnace Preparation: Thermco Products Co., three-inch.
   a. Oxidation Tube: 1050° C; N_2, dry O_2, and wet O_2 at one atmosphere pressure, one liter per minute flow rate.
   b. P-type Tube: 1050° C; N_2, dry O_2, and wet O_2 at one atmosphere pressure, one liter per minute flow rate.
   c. N-type Tube: 1000° C; N_2, dry O_2, and wet O_2 at one atmosphere pressure, one liter per minute flow rate.
4. Initial Oxide: 4000 angstroms.
   a. Initial Wafer Cleaning: Standard Processing Clean.
   b. Oxidation tube.
   c. Cycle Times: 20 minutes dry O_2, 30 minutes wet O_2, 20 minutes dry O_2, and 18 hours N_2.
   d. Push/pull: First two feet in/last two feet out at one foot per minute.
   e. Measure Oxide with Ellipsometer: First and last wafers in boat.

f. Remove oxide grown on control wafer using undiluted HF.

5. Isolation Diffusion: Boron Source.

a. Surface Cleaning: Standard Processing Clean.

b. Isolation mask photolithography process.

c. Etch Isolation Pattern: Cleaning/etching solution CL4.

d. P-type Tube: Predeposition.

e. Cycle Time: 40 minutes Dry N_2.

f. Push/pull: First two feet in/last two feet out at one foot per minute.

g. Remove Borosilicate Glass: Cleaning/etching solution CL2.

h. Surface Cleaning: Standard Processing Clean.

i. P-type Tube: Drive

j. Cycle Time: 90 minutes dry N_2.

k. Push/pull: First two feet in/last two feet out at one foot per minute.

l. Check oxide thickness grown on control wafer.

6. Gate Diffusion: Boron Source.

a. Surface Cleaning: Standard Processing Clean.

b. Gate mask photolithography process.

c. Etch Gate Pattern: Cleaning/etching solution CL4.

d. P-type Tube: Predeposition.

e. Cycle Time: 12 minutes Dry N_2.

f. Push/pull: First two feet in/last two feet out at one foot per minute.

g. Remove Borosilicate Glass: Cleaning/etching solution CL2.

h. Four-point Probe: Check predep resistivity on control wafer.

i. Surface Cleaning: Standard Processing Clean.

j. P-type Tube: Drive and gate oxide.

k. Cycle Time: 4 minutes dry O_2, 27 minutes wet O_2, and 3 minutes dry O_2.

l. Push/pull: First two feet in/last two feet out at one foot per minute.

m. Four-point Probe: Check drive resistivity on control wafer.

n. Check field oxide thickness grown on control wafer.

o. Remove oxide grown on control wafer using undiluted HF.

7. Source/drain Diffusion: Phosphorous Source.

a. Surface Cleaning: Standard Processing Clean.

b. Source/drain mask photolithography process.

c. Etch Source/Drain Pattern: Cleaning/etching solution CL4.

d. N-type Tube: Predeposition.

e. Cycle Time: 15 minutes Dry N_2.

f. Push/pull: First two feet in/last two feet out at one foot per minute.

g. Four-point Probe: Check predep resistivity on control wafer.

h. Surface Cleaning: Standard Processing Clean.

i. N-type Tube: Drive and source/drain oxide.

j. Cycle Time: 3 minutes dry O_2, 5 minutes wet O_2, 1 minutes dry O_2.

k. Push/pull: First two feet in/last two feet out at one foot per minute.

8. Contact Window Openings:

a. Surface Cleaning: Cleaning/etching solution CL3.

b. Contact window mask photolithography process.

c. Etch Contact Window Pattern: Cleaning/etching solution CL4.

9. Metallization: Consolidated Vacuum Corp. vacuum chamber.

a. Surface Cleaning: Cleaning/etching solution CL3.

b. Metallization mask photolithography process.

c. 500 angstroms aluminum.

d. 500 angstroms silver.

e. Metal lift off.

APPENDIX K

STANDARD PROCESSING CLEAN

This cleaning procedure is performed on the wafers prior to each time they are placed in the diffusion furnace to reduce the diffusion of surface contaminants into the wafer and to avert contamination of the furnace tubes.

1. Mix SC1 and immediately immerse wafers for 15 minutes.
2. Rinse wafers in DIW above 10 megohms for 5 minutes.
3. Dip wafers in 10:1 HF for 15 seconds.
4. Rinse wafers in DIW above 10 megohms for 5 minutes.
5. Immerse wafers in SC2 for 15 minutes.
6. Rinse wafers in DIW above 10 megohms for 5 minutes.

STANDARD CLEAN 1 (SC1):

This cleaning solution is composed of hydrogen peroxide (H_2SO_4) and hydrogen peroxide (H_2O_2), and is used to remove organic contaminants from the wafer surface.

1:1, H_2SO_4:H_2O_2

The combination of the two constituent chemicals cause an exothermic reaction and generates a bubbling action. The reaction lasts only about 15 minutes and the solution is fairly ineffective as a clean after this time.

10:1 HF:

This cleaning solution is used to remove the oxide grown on the surface of the wafer during the SC1 immersion

and any oxide which may have grown during exposure to air at room temperature. It is composed of hydrofluoric acid (HF) diluted with deionized water (DIW).

10:1, DIW:HF

STANDARD CLEAN 2 (SC2):

This cleaning solution is used to remove any ionic contaminants left on the surface by the HF dip or any metals picked up by the wafer during handling. It is composed of hydrochloric acid (HCl), H_2O_2, and DIW. The solution must be maintained at 70° C during use.

5:1:1, DIW:HCl:H_2O_2

APPENDIX L

POLYIMIDE/NEGATIVE PR ENCAPSULATION PROCESS FOR WAFERS

This schedule outlines a consistent photolithography process using polyimide and negative photoresist on 3-1/2 inch practice wafers. Prior to applying an additional coat, the polyimide must be fully cured.

1. Clean wafers using Standard Clean process and 220° C oven.
2. Preheat second oven to 70° C.
3. Remove wafer from 220° C oven after bakeout and allow to cool.
4. Blow clean with N_2 - removes surface dust.
5. Apply polyimide adhesion promoter (VM-651):
   - puddle on wafer.
   - spin/spread @ 2 krpm for 10 sec.
   - spin @ 5 krpm for 30 sec.
6. Apply polyimide (PI 2555):
   - puddle on wafer.
   - spin/spread @ 2 krpm for 5 sec.
   - spin @ 6.5 krpm for 30 sec.
7. Prebake PI 2555 at 70° C for 20 minutes, N_2 ambient - dries the polyimide without curing; place in oven immediately to minimize formation of pinholes.
8. Remove from oven, and allow to cool.
9. Blow with N_2 - removes surface dust.
10. Apply negative photoresist (Waycoat Type 3, 28 CP):
    - puddle on wafer.
    - spin/spread @ 5 krpm for 30 sec.
11. Prebake photoresist at 70° C for 20 minutes, N_2 ambient.
12. Blow clean with N_2.
13. Align/expose - 4.5 seconds.

14. Develop photoresist:
    - spin/spray Xylene @ 1 krpm for 20 sec (spray enough to keep wet).
    - spin/spray Butyl Acetate @ 1 krpm for 20 sec.
    - spin/blow N_2 @ 1 krpm for 30 sec.

15. Examine pattern to determine if additional developing required.

16. Postbake at 120° C for 20 minutes, N_2 ambient - toughens photoresist.

17. Etch the polyimide:
    - AZ351 (1:5) bath - 5 sec.
    - DIW bath - 30 sec.
    - Blow dry with N_2.

18. Examine - check for full etch without PR lifting or pattern breaking; reaccomplish etch, if required.

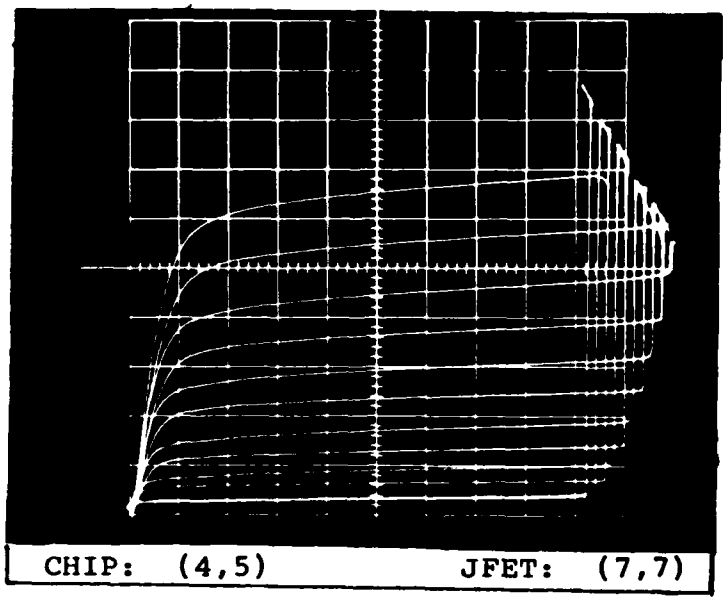
19. Cure at 180° C for 2 hours, N_2 ambient - full cure prior to an additional coat.

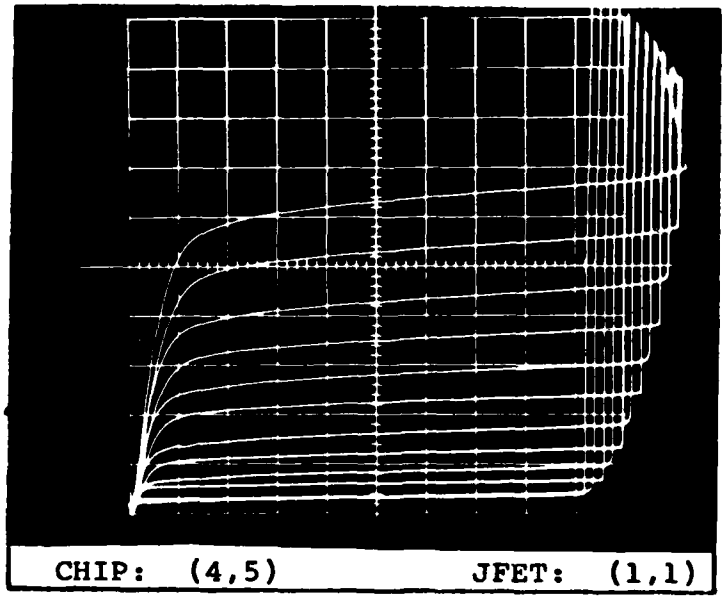
Taken From (Ref 7)

APPENDIX M

JFET V-I CHARACTERISTIC COMPARISONS

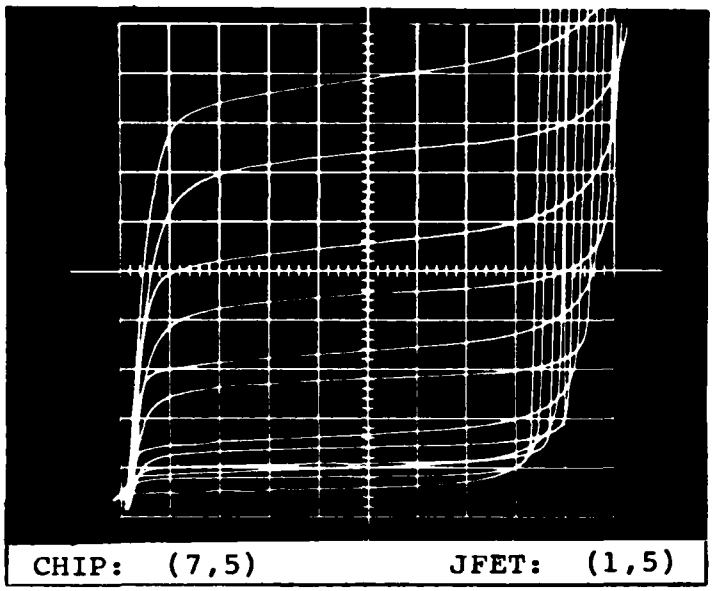
Comparison of JFETs from Same Chip

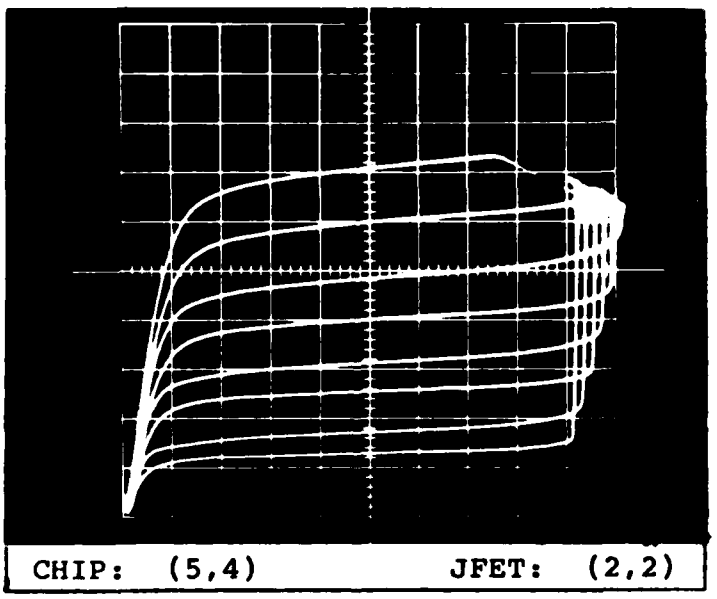




Vertical Scale: 0.02 mA/DIV Horizontal Scale: 0.5 V/DIV
Gate Step Voltage: -0.1 V/STEP
Source & Substrate Grounded

Comparison of JFETs from Different Chips





Vertical Scale: 0.02 mA/DIV Horizontal Scale: 0.5 V/DIV
Gate Step Voltage: -0.1 V/STEP
Source & Substrate Grounded

VITA

Michael Edward Sopko was born on 30 March 1961 in San Juan, Puerto Rico. He graduated from West Hazleton High School, West Hazleton, Pennsylvania in 1979. He attended Wilkes College, Wilkes-Barre, Pennsylvania on a four-year ROTC scholarship, from which he received the degree of Bachelor of Science in Electrical Engineering in May 1983. Through the ROTC program he was commissioned into the United States Air Force upon graduation. He entered the Air Force Institute of Technology, School of Engineering, as his first assignment in June 1983.

Permanent address: 15 North Parkview Drive
Tresckow, Pennsylvania 18254

UNCLASSIFIED
SECURITY CLASSIFICATION OF THIS PAGE

AD-A151 803

REPORT DOCUMENTATION PAGE

1a. REPORT SECURITY CLASSIFICATION UNCLASSIFIED	1b. RESTRICTIVE MARKINGS
2a. SECURITY CLASSIFICATION AUTHORITY	3. DISTRIBUTION/AVAILABILITY OF REPORT Approved for public release; Distribution unlimited
2b. DECLASSIFICATION/DOWNGRADING SCHEDULE	
4. PERFORMING ORGANIZATION REPORT NUMBER(S) AFIT/GE/EE/84D-63	5. MONITORING ORGANIZATION REPORT NUMBER(S)
6a. NAME OF PERFORMING ORGANIZATION School of Engineering 6b. OFFICE SYMBOL (If applicable) AFIT/ENG	7a. NAME OF MONITORING ORGANIZATION
6c. ADDRESS (City, State and ZIP Code) Air Force Institute of Technology Wright-Patterson AFB, Ohio 45433	7b. ADDRESS (City, State and ZIP Code)
8a. NAME OF FUNDING/SPONSORING ORGANIZATION Air Force Aerospace Medical Research Laboratory 8b. OFFICE SYMBOL (If applicable) AFAMRL/HEG	9. PROCUREMENT INSTRUMENT IDENTIFICATION NUMBER
8c. ADDRESS (City, State and ZIP Code) Air Force Aerospace Medical Research Laboratory Human Engineering Division AFAMRL/HEG, Wright-Patterson AFB, Ohio 45433	10. SOURCE OF FUNDING NOS. PROGRAM ELEMENT NO. / PROJECT NO. / TASK NO. / WORK UNIT NO.
11. TITLE (Include Security Classification) See Block 19	
12. PERSONAL AUTHOR(S) Michael E. Sopko, B.S., 2Lt, USAF	
13a. TYPE OF REPORT MS Thesis 13b. TIME COVERED FROM _____ TO _____	14. DATE OF REPORT (Yr., Mo., Day) 1984 December 15. PAGE COUNT 159
16. SUPPLEMENTARY NOTATION	

17. COSATI CODES			18. SUBJECT TERMS (Continue on reverse if necessary and identify by block number)
FIELD	GROUP	SUB. GR.	
09	01		JFET; NMOS; Multiplexed; Multielectrode Array.

19. ABSTRACT (Continue on reverse if necessary and identify by block number)

Title: FABRICATION OF A BIOLOGICALLY-IMPLANTABLE, MULTIPLEXED, MULTIELECTRODE ARRAY OF JFETS FOR CORTICAL IMPLANTATION

Thesis Chairman: Roger D. Colvin, Capt, USAF

Approved for public release: IAW AFR 190-17
21 Feb 85
LYNN E. WOLAVER
Dean for Research and Professional Development
Air Force Institute of Technology (AIC)
Wright-Patterson AFB OH 45433

20. DISTRIBUTION/AVAILABILITY OF ABSTRACT	21. ABSTRACT SECURITY CLASSIFICATION
UNCLASSIFIED/UNLIMITED ☒ SAME AS RPT. ☐ DTIC USERS ☐	UNCLASSIFIED

22a. NAME OF RESPONSIBLE INDIVIDUAL	22b. TELEPHONE NUMBER (Include Area Code)	22c. OFFICE SYMBOL
Roger D. Colvin, Capt, USAF	(513)-255-3450	AFIT/ENG

DD FORM 1473, 83 APR EDITION OF 1 JAN 73 IS OBSOLETE.

UNCLASSIFIED
SECURITY CLASSIFICATION OF THIS PAGE

A new JFET multielectrode array, comprised of a 16 by 16 array of 256 junction field effect transistors, has been fabricated for use a cortical implant. Changes in the fabrication procedure include: The use of a new chrome, six layer mask set, in lieu of emulsion masks; different diffusion times and temperatures; implementation of HCl gettering and backside gettering techniques; and a revised processing schedule incorporating different wafer cleaning procedures.

The primary emphasis of this ~~study~~ was on the development of a viable processing schedule for fabrication of the array. Secondary emphasis was placed upon interfacing the array to an NMOS multiplexer and a proposed method of mounting the device in a cortically implantable package.

END

FILMED

5-85

DTIC